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TFT | OLED | CHARACTER | GRAPHIC | UWVD | SEGMENT | CUSTOM

Graphic Display Module

Part Number

G12864A-KB-LW63

Overview:

- 128x64 Graphic LCD
- FSTN Black Negative
- 89.7x49.8mm Module
- Parallel and Serial Interfaces
- Blue LED Backlight
- Transmissive
- Wide Temp Range
- 3.5V
- LCD IC: NT7534
- RoHS Compliant

Graphic LCD Features

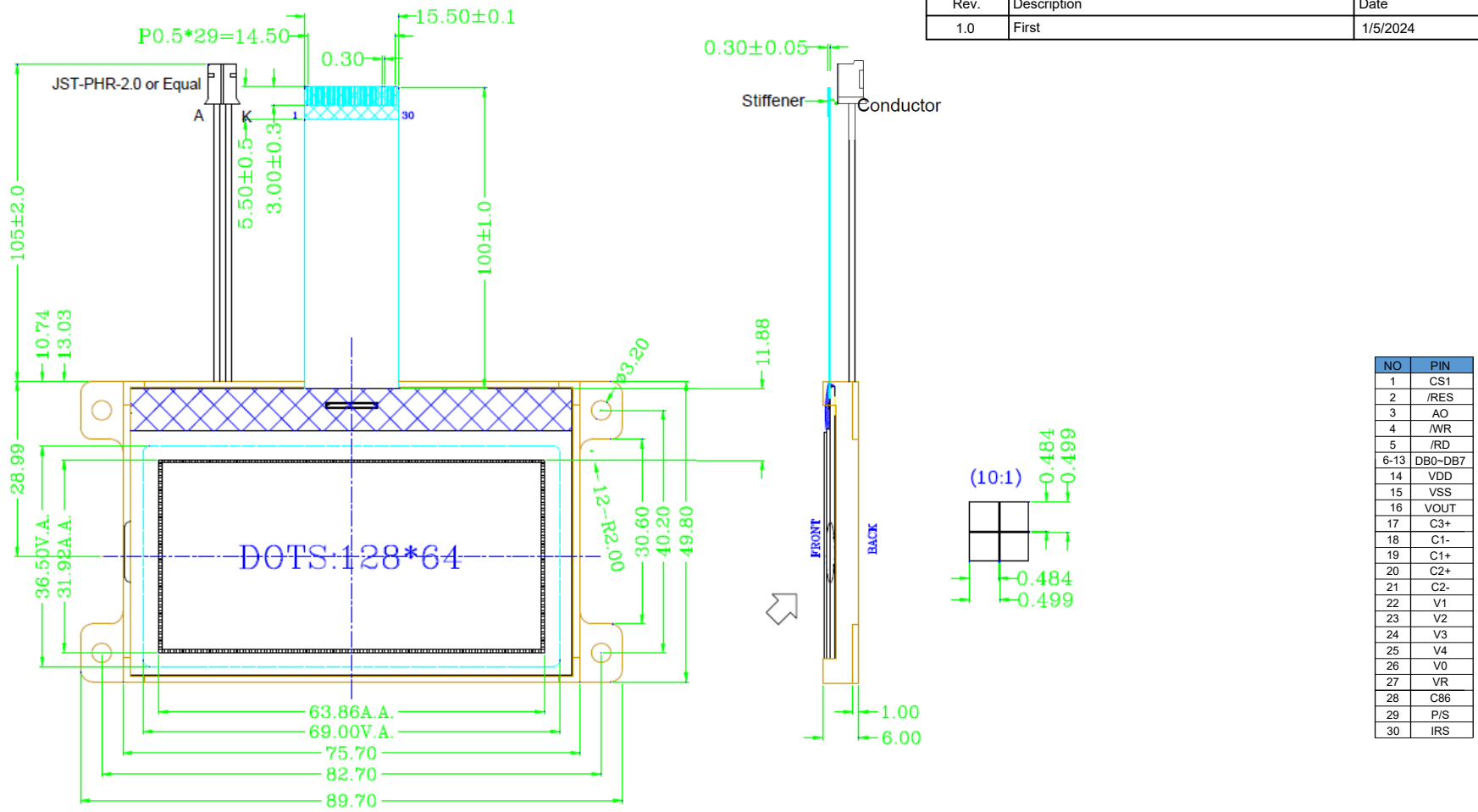
Resolution: 128x64 Dots
Interface(s): 8-bit Parallel (6800/8800), 4SPI interfaces
RoHS Compliant.

General Information Items	Specification	Unit	Note
	Main Panel		
Viewing Area (VA)	69.00 (H) x 36.50 (V)	mm	--
LCD Type	FSTN Negative	--	--
Viewing Angle	6:00	O'Clock	--
Polarizer	Transmissive	--	--
Backlight Type	LED	--	--
Backlight Color	Blue	--	--
LCD IC	NT7534	--	--
Drive Mode	1/64 Duty, 1/9 Bias	--	--
Operating Temperature	-20 to +70	°C	--
Storage Temperature	-30 to +80	°C	--

Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	--	89.70	--	mm	--
	Vertical (V)	--	49.80	--	mm	--
	Depth (D)	--	6.00	--	mm	--
Weight		--	33.0	--	g	Approximate

1. Outline Dimensions



Rev.	Description	Date
1.0	First	1/5/2024

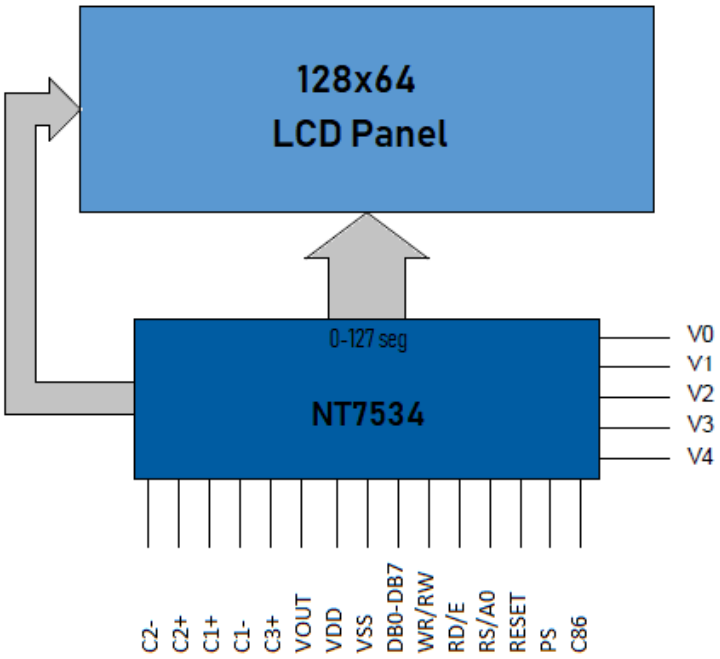
NO	PIN
1	CS1
2	/RES
3	AO
4	/WR
5	/RD
6-13	DB0~DB7
14	VDD
15	VSS
16	VOUT
17	C3+
18	C1-
19	C1+
20	C2+
21	C2-
22	V1
23	V2
24	V3
25	V4
26	V0
27	VR
28	C86
29	P/S
30	IRS

Notes:

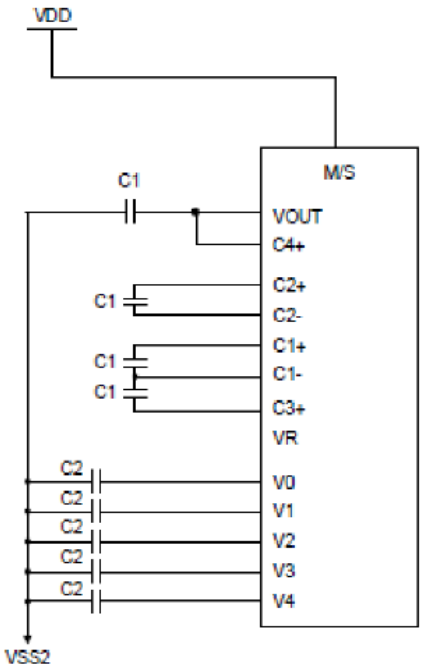
1.) Driver Method: 1/64duty, 1/9bias, VDD 3.0V VLCD 9.8V
2). Display Type: FSTN/Negative/Transmissive
3). Viewing Angle: 6:00
4). Operating Temp: -20°C-70°C
5). Storage Temp: -30°C-80°C
6). Driver: NT7534
7). Backlight Type: Blue LED Vf=3.5V/If=60mA
8). RoHS Compliant

Model Name: G12864A-KB-LW63		FOCUS LCDs LCDs MADE SIMPLE®	
General Tol: ±0.3			
Approvals	Date	Drawing No.:	Scale:
DWN:			
CHK:		Size:	Unit: mm / Page: 1/1
APP:			

2. Block Diagrams



Capacitance 1uF-2.2uF



C1: 1uF-4.7uF for Voltage rating from 10-35V
C2: 1uF-2.2uF for Voltage rating from 6.3-25V

NOTE: See IC controller spec NT7534 for more information on internal voltage regulating circuits. Additional information on DC-DC voltage regulating circuits for graphic LCD's is available on our website at [www.FocusLCDs.com.](http://www.FocusLCDs.com)

3. Input Terminal Pin Assignment

NO.	Symbol	Description	I/O
1	CS1	Chip select in serial interface; low is active.	MPU
2	/RES	When /RES is set to "L", the settings are initialized. The reset operation is performed by the /RES signal level.	MPU
3	A0	Selects registers. 0: instruction; 1: data register.	MPU
4	/WR	Read/write select signal.	MPU
5	/RD	Operation (data read/write) enable signal.	MPU
6-11	DB0~DB5	Display Data.	MPU
12	DB6 (SCL)	Display Data (or Serial Data Clock Signal Input).	MPU
13	DB7 (SI)	Display Data (or Serial Data Input).	MPU
14	VDD	Power supply for logic for LCM.	P
15	VSS	Signal ground for LCM.	P
16	VOUT	DC/DC voltage converter output.	P
17	C3+	For voltage booster circuit. External capacitor about 0.1uF~2.2uF.	P
18	C1-		
19	C1+		
20	C2+		
21	C2-		
22	V1		
23	V2	Power Supply for LCD.	P
24	V3		
25	V4		
26	V0		
27	VR	Voltage adjustment pin. Applies voltage between V0 and VSS using a resistive divider.	MPU
28	C86	This is the MPU interface switch pin. When C86="H": 6800 series MPU interface. When C86="L": 8800 series MPU interface.	MPU
29	P/S	This is the parallel data input / serial data input switch pin. When P/S="H": Parallel data input. When P/S="L": Serial data input.	MPU
30	IRS	This pin selects the reistors for the V0 voltage level adjustment.	MPU

4. LCD Optical Characteristics

FSTN type display module (Ta=25°C, V_{DD}=3.0V)

Item		Symbol	Condition	Min	Typ.	Max	Unit
Contrast Ratio		CR		--	6	--	
Response Time	On	T_{on}		--	150	250	ms
	Off	T_{off}		--	150	250	ms
Viewing Angle $C_R \geq 2$, 25°C	Hor.	Θ_L	CR ≥ 2	-60	--	35	degree
		Θ_R		-60	--	35	
	Ver.	Θ_T		-40	--	40	
		Θ_B		-40	--	40	

5. Electrical Characteristics

5.1 Absolute Maximum Rating

Characteristics	Symbol	Min	Max	Unit
Power Voltage Logic	V_{DD}	0.3	3.6	V
Input Voltage	V_{IN}	-0.3	V_{DD} + 0.3	V
Power Supply for LCD	V_0 - V_{ss}	-0.3	14.2	V
Operating Temperature	T_{OP}	-20	+70	°C
Storage Temperature	T_{ST}	-30	+80	°C

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage for LCD	V_0-V_{ss}	Ta = 25°C	9.3	9.8	12.7	V
Supply Voltage for Logic	V_{DD}		2.8	3.0	3.3	V
Supply Current	I_{DD}	Ta = 25°C, V_{DD} = 3.0V	--	1.1	1.6	mA
Backlight Supply Voltage	V_F		2.8	3.0	3.2	V
Backlight Supply Current	I_{LED}	V_F = 3.5V	30	60	90	mA

Condition:

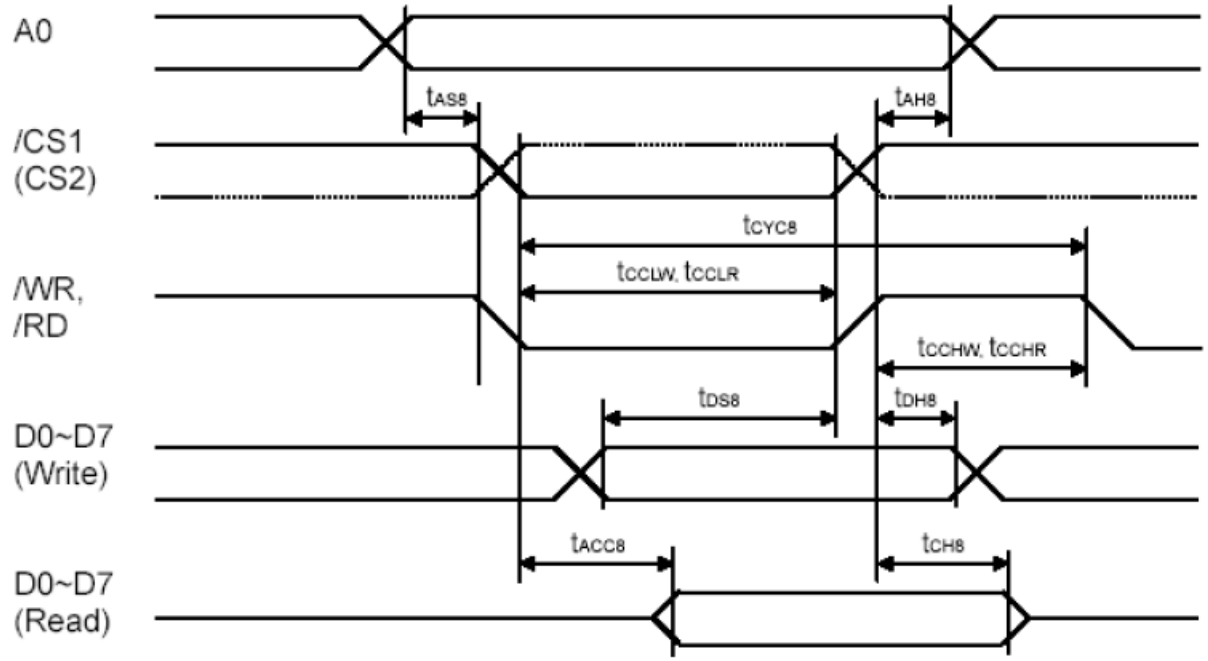
1. VDD = 3.0V
2. 1/64 Duty, 1/9 Bias

6. Signal Timing Characteristics

6.1 8-bit Parallel Timing Characteristics (8080-series)

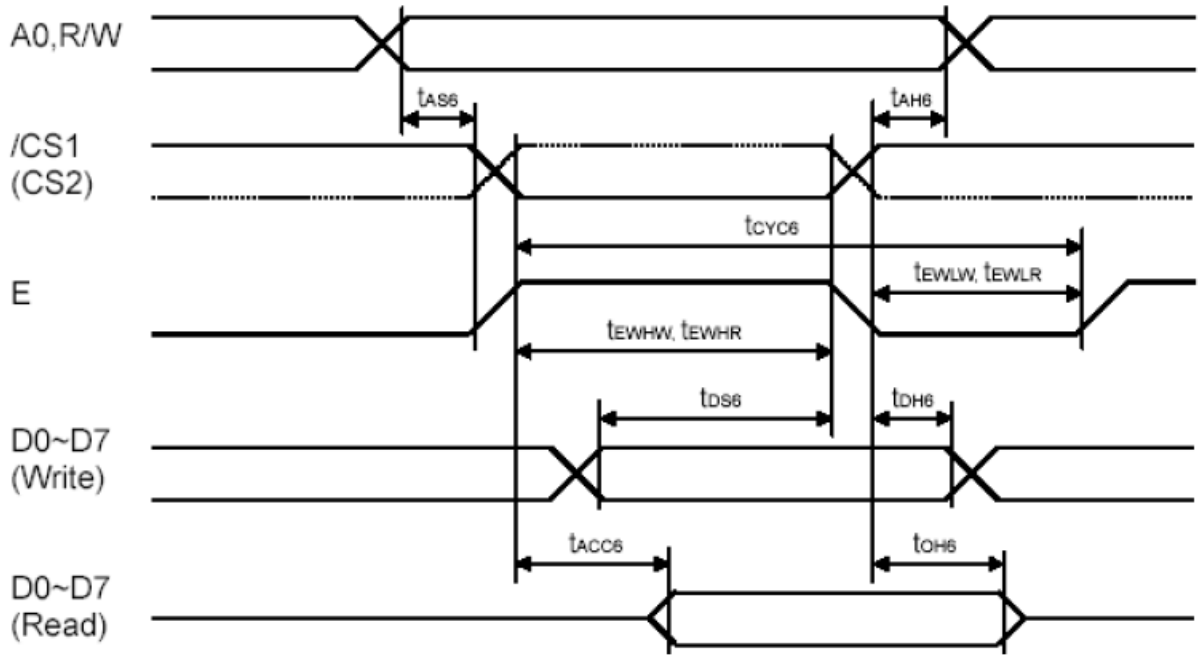
Parameter	Signal	Symbol	Min	Max	Unit	Note
Address hold time	A0	t_{AH8}	0	--	ns	
Address setup time		t_{AS8}	0	--	ns	
Address cycle time		t_{CYC8}	240	--	ns	
Enable L pulse width (write)	WR	t_{CCLW}	90	--	ns	
Enable H pulse width (write)		t_{CCHW}	100	--	ns	
Enable L pulse width (read)	RD	t_{CCLR}	120	--	ns	
Enable H pulse width (read)		t_{CCHR}	60	--	ns	
Write data setup time	DB0-DB7	t_{DS8}	40	--	ns	
Write address hold time		t_{DH8}	10	--	ns	
Read access time		t_{ACC8}	--	140	ns	CL=100pF
Read output disable time		t_{CH8}	5	50	ns	CL=100pF

System Buses Read/Write Characteristics (for 8080 Series MPU)



6.2 8-bit Parallel Timing Characteristics (6800-series)

Parameter	Signal	Symbol	Min	Max	Unit	Note
Address hold time	A0	t_{AH6}	0	--	ns	
Address setup time		t_{AS6}	0	--	ns	
Address cycle time		t_{CYC6}	240	--	ns	
Enable L pulse width (write)	WR	t_{EWLW}	100	--	ns	
Enable H pulse width (write)		t_{EWHW}	90	--	ns	
Enable L pulse width (read)	RD	t_{EWLR}	60	--	ns	
Enable H pulse width (read)		t_{EWHR}	120	--	ns	
Write data setup time	DB0-DB7	t_{DS6}	40	--	ns	
Write address hold time		t_{DH6}	10	--	ns	
Read access time		t_{ACC6}	--	140	ns	CL=100pF
Read output disable time		t_{OH6}	5	50	ns	CL=100pF

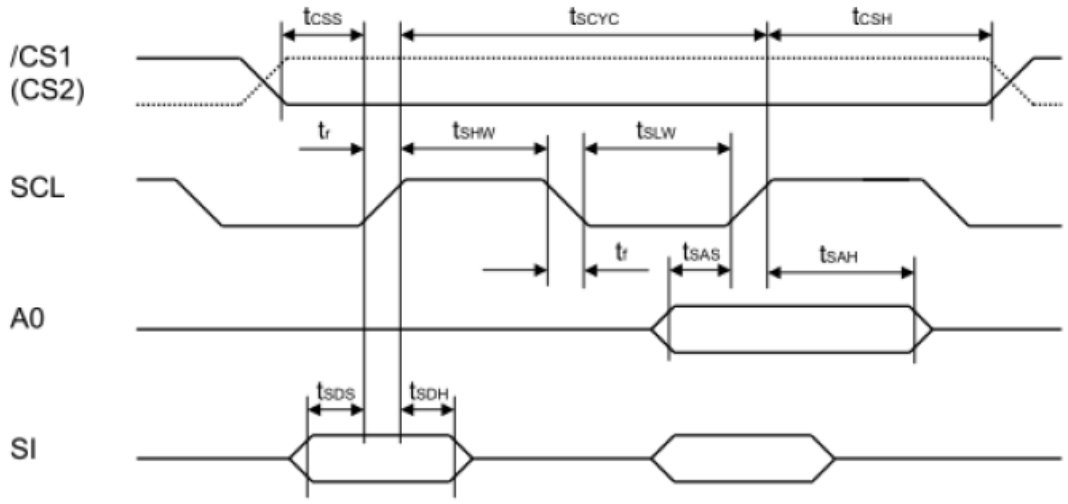


6.3 Serial Interface

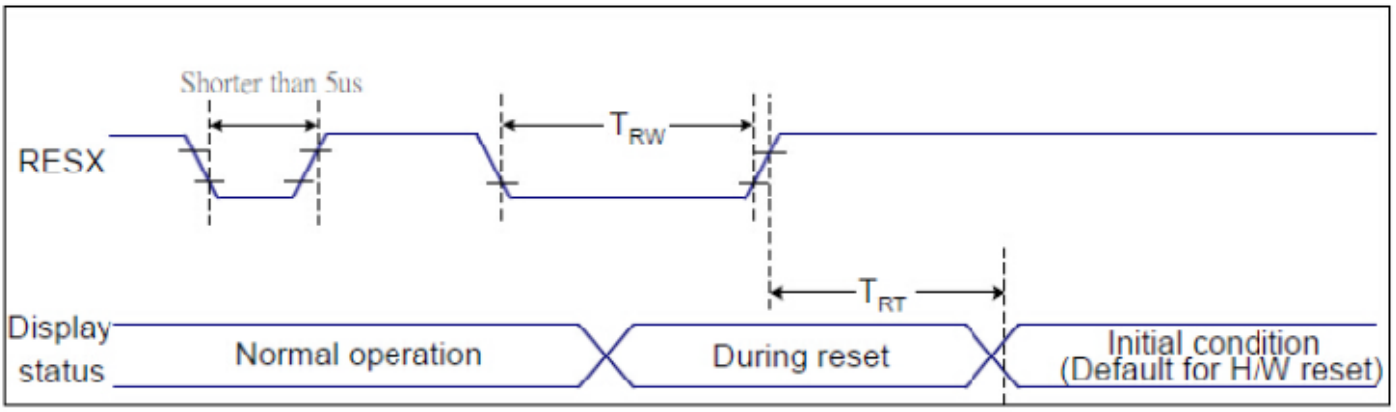
(VDD=3.0V, Ta=25˚C)

Parameter	Signal	Symbol	Min	Max	Unit	Note
Serial Clock Period	SCL	TSCYC	120	--	ns	
SCL "H" pulse width		TSHW	60	--	ns	
SCL "L" pulse width		TSLW	60	--	ns	
Address setup time	A0	TSAS	30	--	ns	
Address hold time		TSAH	20	--	ns	
Data setup time	SI	TSDS	30	--	ns	
Data hold time		TSDH	20	--	ns	
Chip select setup time	CS	TCSS	20	--	ns	
Chip select hold time		TCSH	40	--	ns	

Serial Interface Timing



6.4 Reset Timing



	Symbol	Parameter	Min	Max	Unit
RESX	t_R	Reset time	-	1.0	us
	t_{RW}	Reset 'L' pulse width	10	-	us

Notes:

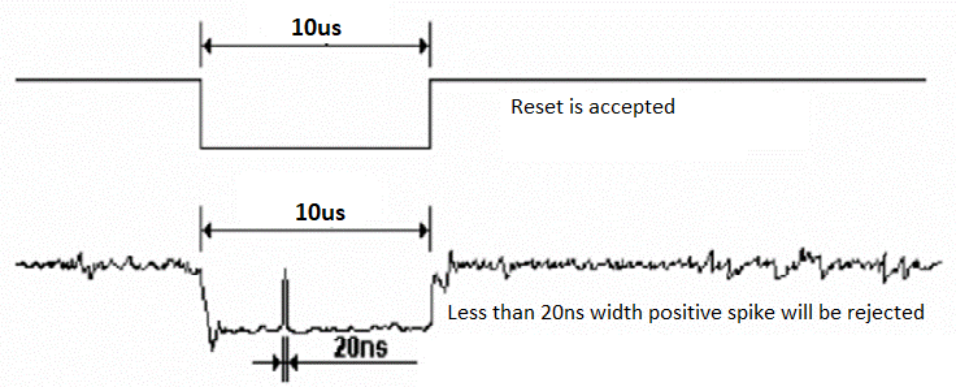
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

7. Command Table

Command	A0	RD	WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Description
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0 1	AEh AFh	Turn on LCD panel when high, and turn off when low
(2) Display Start Line Set	0	1	0	0	1	Display Start Address						40h to 7Fh	Specifies RAM display line for COM0
(3) Page Address Set	0	1	0	1	0	1	1	Page Address				B0h to B8h	Set the display data RAM page in Page Address register
(4) Column Address Set	0	1	0	0	0	0	1	Higher Column Address				00h to 18h	Set 4 higher bits and 4 lower bits of column address of display data RAM in register
	0	1	0	0	0	0	0	Lower Column Address					
(5) Read Status	0	0	1	Status				0	0	0	0	XX	Reads the status information
(6) Write Display Data	1	1	0	Write Data								XX	Write data in display data RAM
(7) Read Display Data	1	0	1	Read Data								XX	Read data from display data RAM
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	A0h A1h	Set the display data RAM address SEG output correspondence
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	A6h A7h	Normal indication when low, but full indication when high
(10)Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	A4h A5h	Select normal display (0) or entire display on
(11)LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0 1	A2h A3h	Sets LCD driving voltage bias ratio
(12)Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	E0h	Increments column address counter during each write
(13)End	0	1	0	1	1	1	0	1	1	1	0	EEh	Releases the Read-Modify-Write
(14)Reset	0	1	0	1	1	1	0	0	0	1	0	E2h	Resets internal functions
(15)Common Output Mode Select	0	1	0	1	1	0	0	0 1	*	*	*	C0h to CFh	Select COM output scan direction *: invalid data
(16)Power Control Set	0	1	0	0	0	1	0	1	Operation Status			28h to 2Fh	Select the power circuit operation mode
(17)V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h to 27h	Select internal resistor ratio Rb/Ra mode
(18)Electronic Volume mode Set	0	1	0	1	0	0	0	0	0	0	1	81h	
Electronic Volume Register Set	0	1	0	*	*	Electronic Control Value						XX	Sets the V0 output voltage electronic volume register
(19)Set Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	ACh ADh	Sets static indicator ON/OFF 0: OFF, 1: ON
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	Mode		XX	Sets the flash mode
(20)Power Save	0	1	0	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21)NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation

8.0 Cautions and Handling Precautions

8.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

8.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.