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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E60RA-I-MW560-N

Overview:

- 6.0-inch TFT (75.04x147.63 mm)
- 720 x 1440
- 4-lane MIPI DSI @
- Full Temperature
- All View
- Transmissive, IPS
- No Touch Panel
- 560 NITS
- TFT IC: ILI9881C
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT-LCD Panel, driver circuit and a backlight unit. The resolution of this 6.0" TFT LCD contains 720(RGB)x1440 pixels and can display up to 16.7M colors.

TFT Features

Low Input Voltage: 3.3V

Display Colors: 16.7M

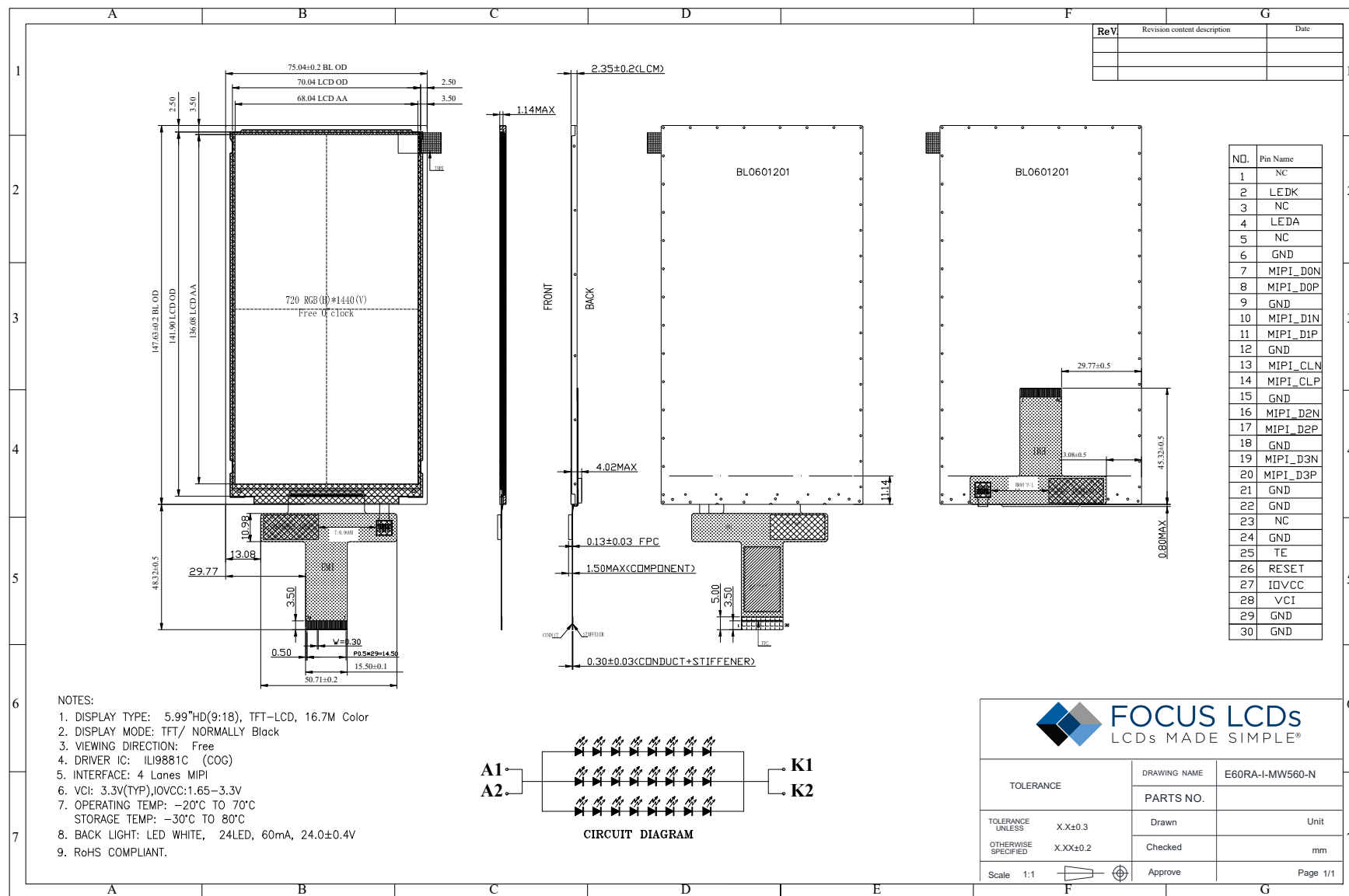
Interface: 4-lane MIPI

General Information Items	Specification	Unit	Note
	Main Panel		
TFT Display area (AA)	68.04(H) x 136.08(V) (6.0 inch)	mm	-
Driver Element	TFT active matrix	-	-
Display Colors	16.7M	colors	-
Number of pixels	720(RGB)x1440	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel Pitch	0.0945 (H)x0.0945(V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ILI9881C	-	-
TFT Interface	4-lane MIPI	-	-
Display mode	Transmissive/ Normally Black	-	-
Operating temperature	-20-+70	°C	-
Storage temperature	-30-+80	°C	-

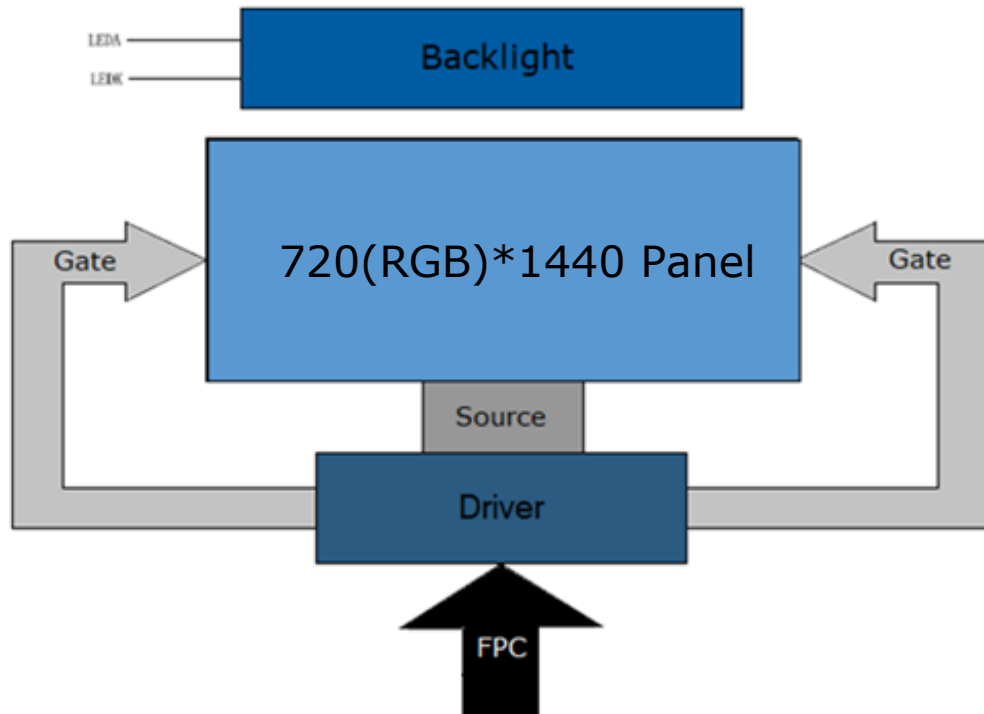
Mechanical Information

Item		Min	Typ.	Max	Unit	Note
Module Size	Horizontal (H)		75.04		mm	-
	Vertical (V)		147.63		mm	-
	Depth (D)		2.35		mm	-
	Weight		52		g	-

1. Outline Dimensions



2. Block Diagram



3. Input Terminal Pin Assignment

Recommended Connector: FH19C-30S-0.5SH(99)

NO.	Symbol	Description	I/O
1	NC	Not connected	
2	LEDK	Cathode pin of the backlight	P
3	NC	Not connected	
4	LEDA	Anode pin of the backlight	P
5	NC	Not connected	
6	GND	Ground	P
7	D0N	MIPI DSI differential data pair lane 0	I/O
8	D0P		
9	GND	Ground	P
10	D1N	MIPI DSI differential data pair lane 1	I/O
11	D1P		
12	GND	Ground	P
13	CLKN	MIPI DSI differential clocking pair	I/O
14	CLKP		
15	GND	Ground	P
16	D2N	MIPI DSI differential data pair lane 2	I/O
17	D2P		
18	GND	Ground	P
19	D3N	MIPI DSI differential data pair lane 3	I/O
20	D3P		
21	GND	Ground	P
22	GND	Ground	P
23	NC	Not connected	
24	GND	Ground	P
25	TE	Tearing effect output pin. Leave open when not used.	O
26	RESET	Reset signal of the device. Initializes the chip, active low.	I
27	IOVCC	Power supply voltage for I/O	P
28	VCI	Power supply voltage for analog circuits	P
29	GND	Ground	P
30	GND	Ground	P

I: Input, O: Output, P: Power

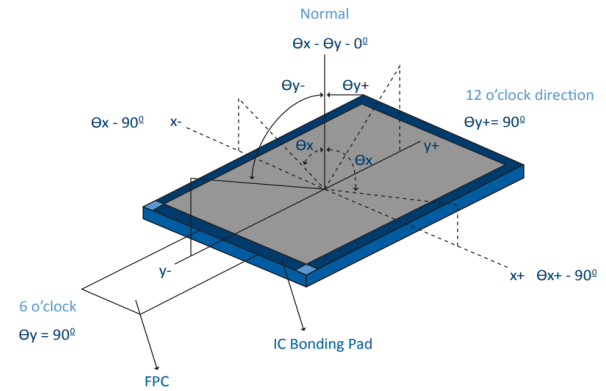
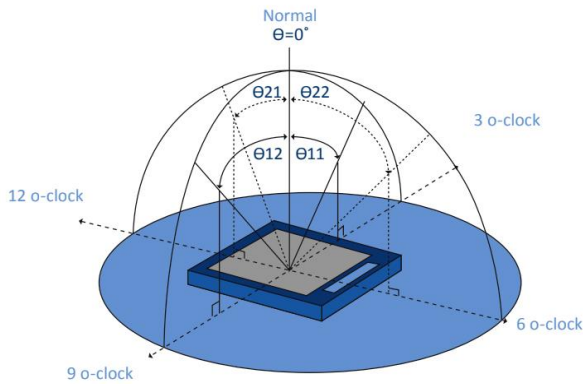
4. LCD Optical Characteristics

4.1 Optical Specifications

Item		Symbol	Condition	Min	Typ.	Max	Unit	Note
Color Gamut		S%	θ=0 Normal viewing angle	65	68	--	%	(3)
Contrast Ratio		CR		800	1000	--	%	(2)
Response Time	Rising	TR+TF		--	30	45	ms	(4)
	Falling							
Color Filter Chromaticity	White	W _X		0.265	0.305	0.325		(5)(6)
		W _Y		0.289	0.329	0.369		
	Red	R _X		0.613	0.633	0.653		
		R _Y		0.317	0.337	0.357		
	Green	G _X		0.293	0.313	0.333		
		G _Y		0.591	0.611	0.631		
	Blue	B _X	0.125	0.145	0.165			
		B _Y	0.056	0.076	0.092			
Viewing Angle	Hor.	ΘL	CR≥10	--	80	--	degrees	(1)(6)
		ΘR		--	80	--		
	Ver.	ΘT		--	80	--		
		ΘB		--	80	--		
Option View Direction		ALL						(1)

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.

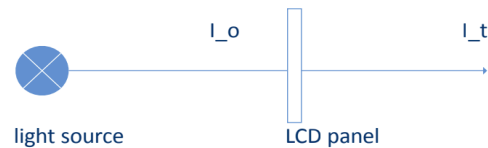


(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving. The equation for transmittance Tr is:

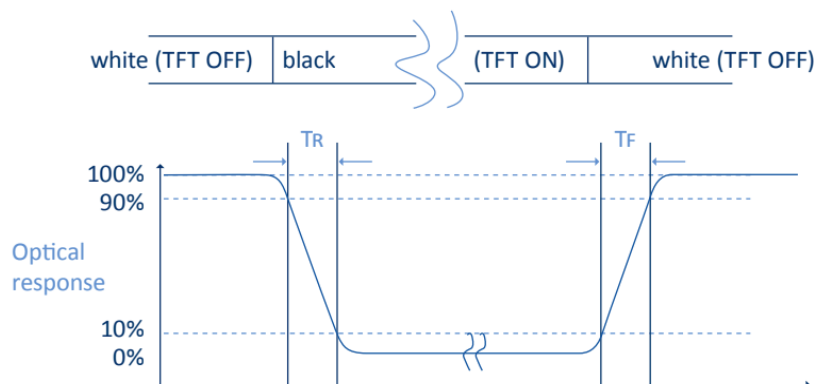
$$Tr = \frac{It}{Io} \times 100\%$$



Io = the brightness of the light source.

It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut:

Measuring machine CFT-01. NTSC's Primaries: $R(x,y,Y)$, $G(x,y,Y)$, $B(x,y,Y)$. FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics. The color chromaticity shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

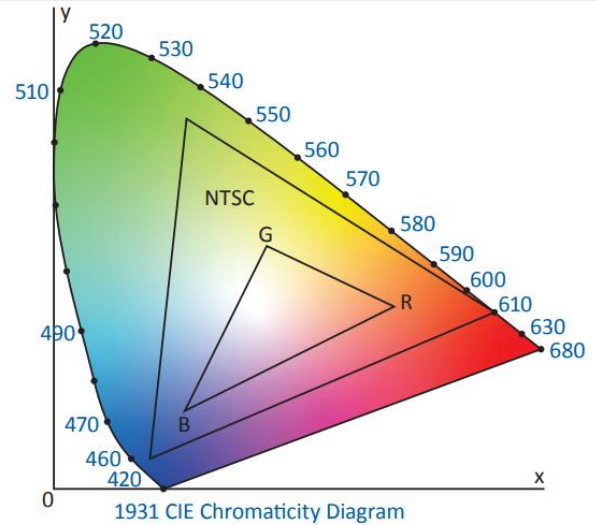
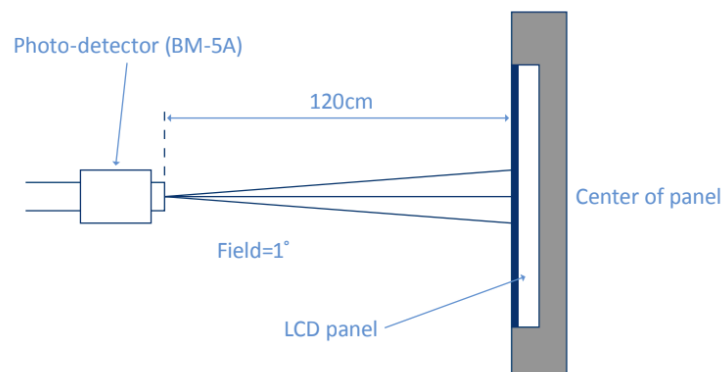
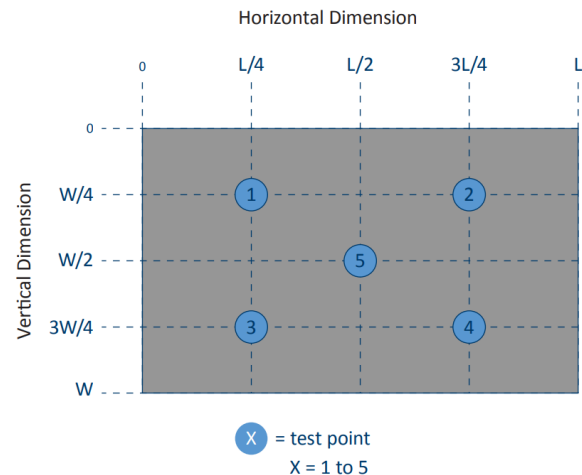
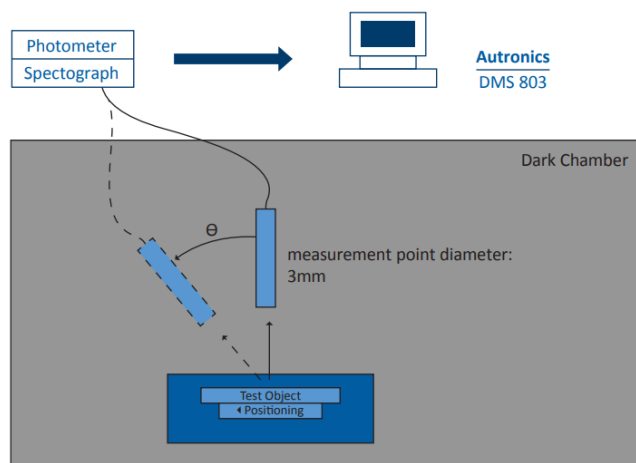


Fig. 1931 CIE chromacity diagram

$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

(6) Definition of Optical Measurement Setup:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.



5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 °C, VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VCI	-0.3	6.5	V
DC/DC Supply Voltage	IOVCC	-0.3	3.3	
Operating Temperature	TOP	-20	+70	°C
Storage Temperature	TST	-30	+80	°C

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Digital Supply Voltage	VCI	2.5	3.3	6.0	V	
Supply Voltage Logic	IOVCC	1.65	1.8	3.3	V	
Normal Mode Current	IDD	--	40	--	mA	
Level Input Voltage	VIH	0.7IOVCC	--	IOVCC	V	
	VIL	-0.3	--	0.3IOVCC	V	
Level Output Voltage	VOH	0.8IOVCC	--	IOVCC	V	
	VOL	GND	--	0.2IOVCC	V	

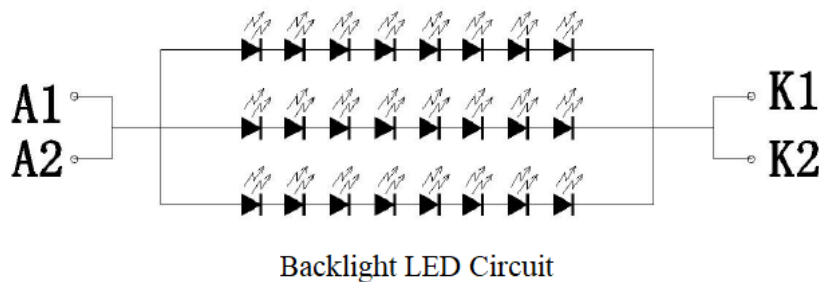
5.3 LED Backlight Characteristics

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	IF	--	60	--	mA	
Forward Voltage	VF	--	24	--	V	
LCM Luminance	LV	540	560	--	cd/m2	Note 3
LED lifetime	Hr	--	50000	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

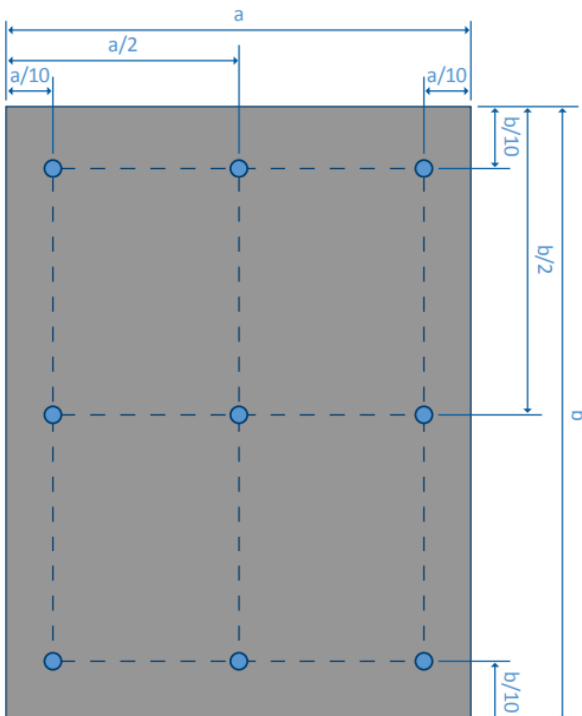
The back-light system is edge-lighting type with 24 white LEDs.

Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 °C, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED lifetime” is defined as the module brightness decrease to 50% original brightness at Ta=25°C and IL=60mA. The LED lifetime could be decreased if operating IL is larger than 60mA. The constant current driving method is suggested.



Note 3: Luminance Uniformity of these 9 points is defined as below:



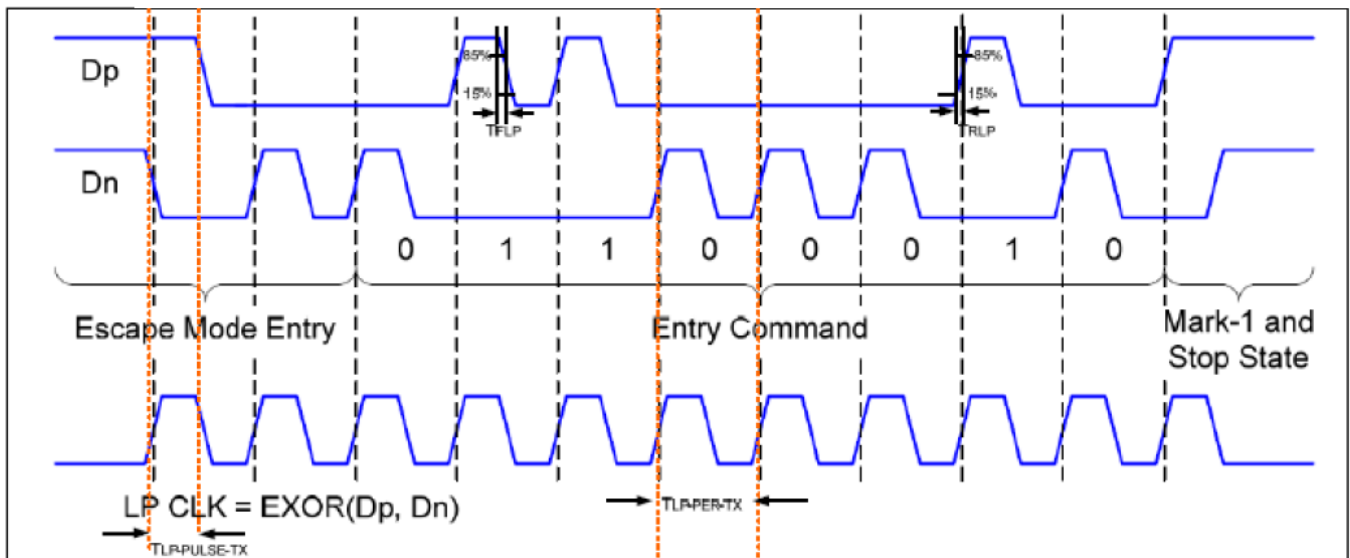
$$\text{Luminance} = \frac{(\text{Total Luminance of 9 points})}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

6. MIPI AC Characteristics

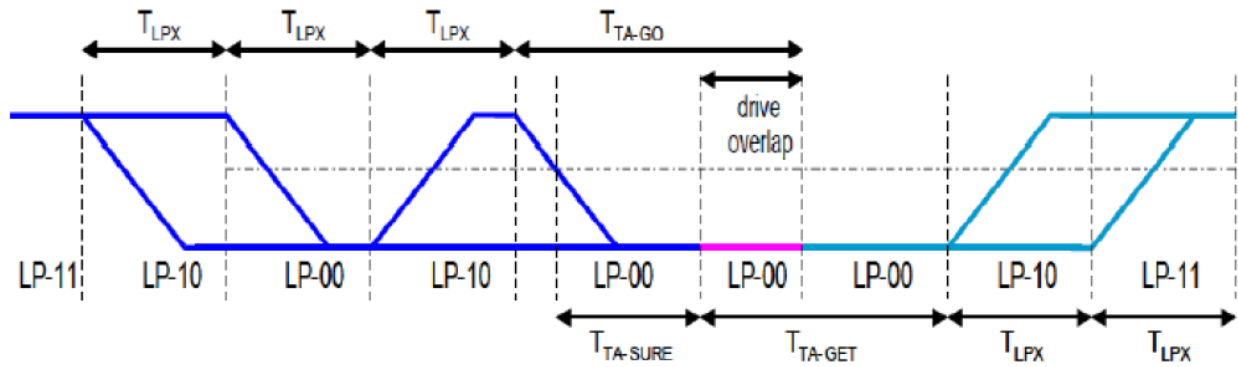
6.1 LP Transmitter AC Specification

Parameter		Symbol	Min	Typ.	Max	Unit	Note
15%-85% rising and falling time		T _{RLP} /T _{FLP}	--	--	25	ns	
30%-85% rising and falling time		T _{REOT}	--	--	35	ns	
Pulse width of LP exclusive OR clock	First LP XOR clock pulse after stop state or last pulse before stop state	T _{LP-PULSE-TX}	40	--	--	ns	
	All other pulses		20	--	--	ns	
Period of the LP XOR clock		T _{LP-PER-TX}	90	--	--	mV/ns	
Slew rate @CLOAD=0pF		dV/dtSR	30	--	500	mV/ns	
Slew rate @CLOAD=5pF			30	--	200	mV/ns	
Slew rate @CLOAD=20pF			30	--	150	mV/ns	
Slew rate @CLOAD=70pF			30	--	100	mV/ns	
Load capacitance		T _{RLP}	--	--	70	pF	



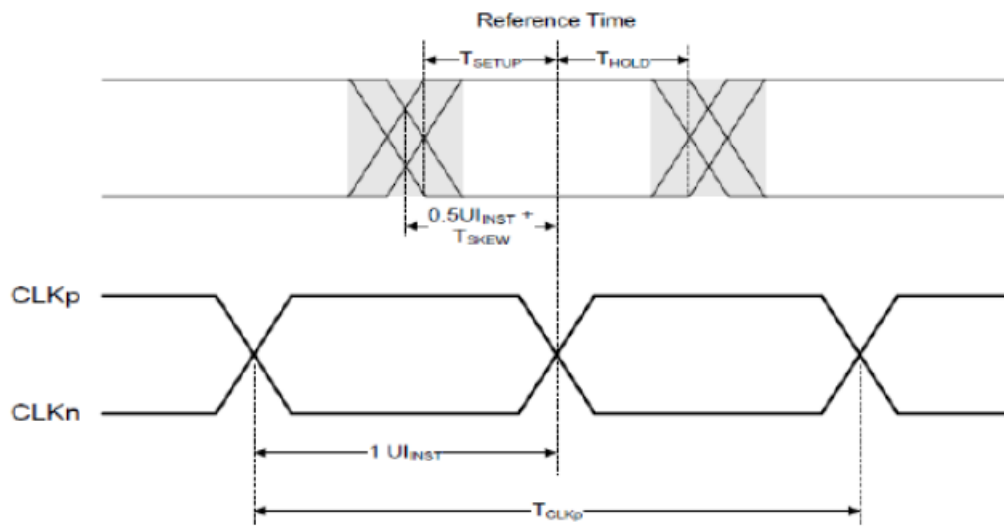
6.2 Turnaround Procedure

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Length of any low power state period: master side	T_{LPX}	50	--	75	ns	
Length of any low power state period: slave side	T_{LPX}	50	55.56	58.34	ns	
Ratio of $T_{LPX}(\text{Master})/T_{LPX}(\text{Slave})$ between master and slave side	$\text{Ratio}T_{LPX}$	2/3	--	3/2	ns	
Time-out before new TX side start driving	$T_{TA-Sure}$	T_{LPX}	--	2 T_{LPX}	ns	
Time to drive LP-00 by new TX	T_{TA-GET}	--	5 T_{LPX}	--	ns	
Time to drive LP-00 after turnaround request	T_{TA-GO}	--	4 T_{LPX}	--	ns	



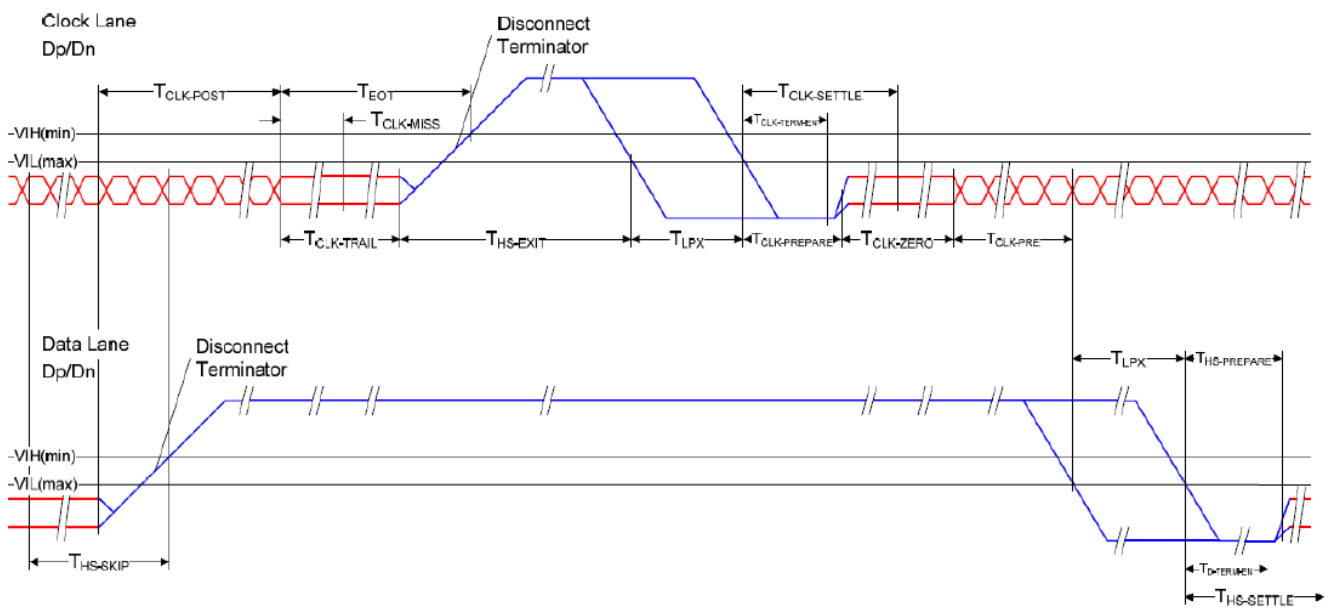
6.3 High Speed Transmission

Parameter	Symbol	Min	Typ.	Max	Unit	Note
UI Instantaneous	UIINST	2	--	12.5	ns	
Data to clock skew (measured at transmitter)	TSKEW(TX)	-0.15	--	0.15	UIINST	
Data to clock setup time (measured at receiver)	TSETUP(RX)	0.15	--	--	UIINST	
Data to clock hold time (measured at receiver)	THOLD(RX)	0.15	--	--	UIINST	
20%-80% rise and fall time	TR, TF	150	--	--	ps	
		--	--	--	UIINST	

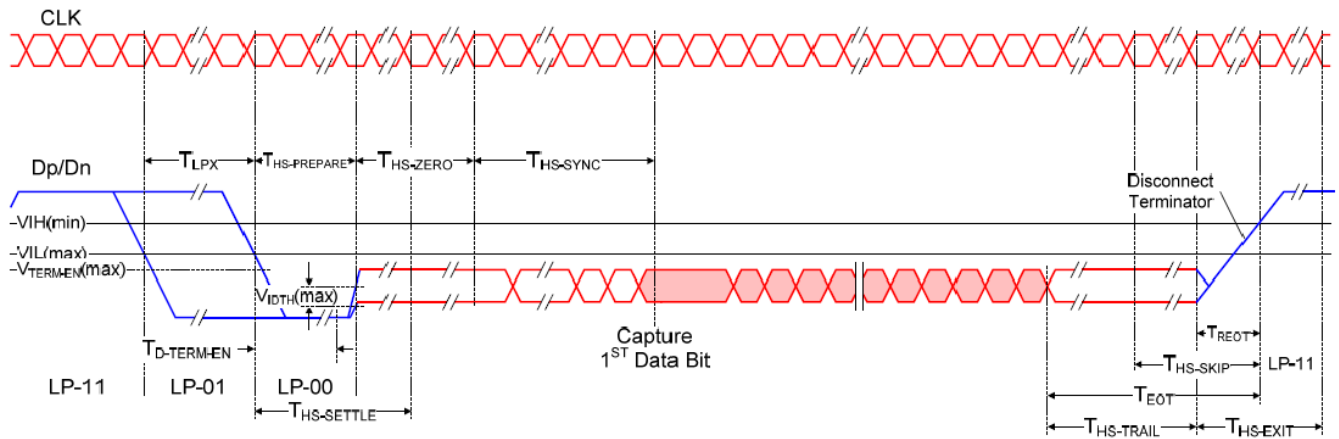


6.4 High Speed Clock Transmission

Parameter	Symbol	Min	Typ.	Max	Unit
Time that the transmitter shall continue sending HS clock after the last associated data lane has transitioned to LP mode	T _{CLK-POST}	60+52UI	--	--	ns
Detection time that the clock has stopped toggling	T _{CLK-MISS}	--	--	60	ns
Time to drive LP-00 to prepare for HS clock transmission	T _{CLK-PREPARE}	38	--	95	ns
Minimum lead HS-0 drive period before starting clock	T _{CLK-PREPARE} +T _{CLK-ZERO}	300	--	--	ns
Time to enable clock lane receiver line termination measured from when Dn crosses VILMAX	T _{HS-TERM-EN}	--	--	38	ns
Minimum time that the HS clock must be prior to any associated data lane beginning the transmission from LP to HS mode	T _{CLK-PRE}	8	--	--	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	T _{CLK-TRAIL}	60	--	--	ns



6.5 High Speed Data Transmission in Bursts



7. Cautions and Handling Precautions

7.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the "Power ON" condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

7.2 Storage and Transportation.

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.