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TFT | OLED | CHARACTER | GRAPHIC | UWVD | SEGMENT | CUSTOM

Character Display Module

Part Number

C204CXBSGSW6WT55XAA

Overview:

- 20x4 Character LCD
- STN Gray
- 77x47 mm Module
- 4-bit or 8-bit MPU Interface(s)
- White LED Backlight
- Transflective
- Wide Temp Range
- 5V
- LCD IC: ST7066U-0A or Equivalent
- RoHS Compliant

Character LCD Features

Characters: 20x4
Interface(s): 4-bit or 8-bit
MPU RoHS Compliant

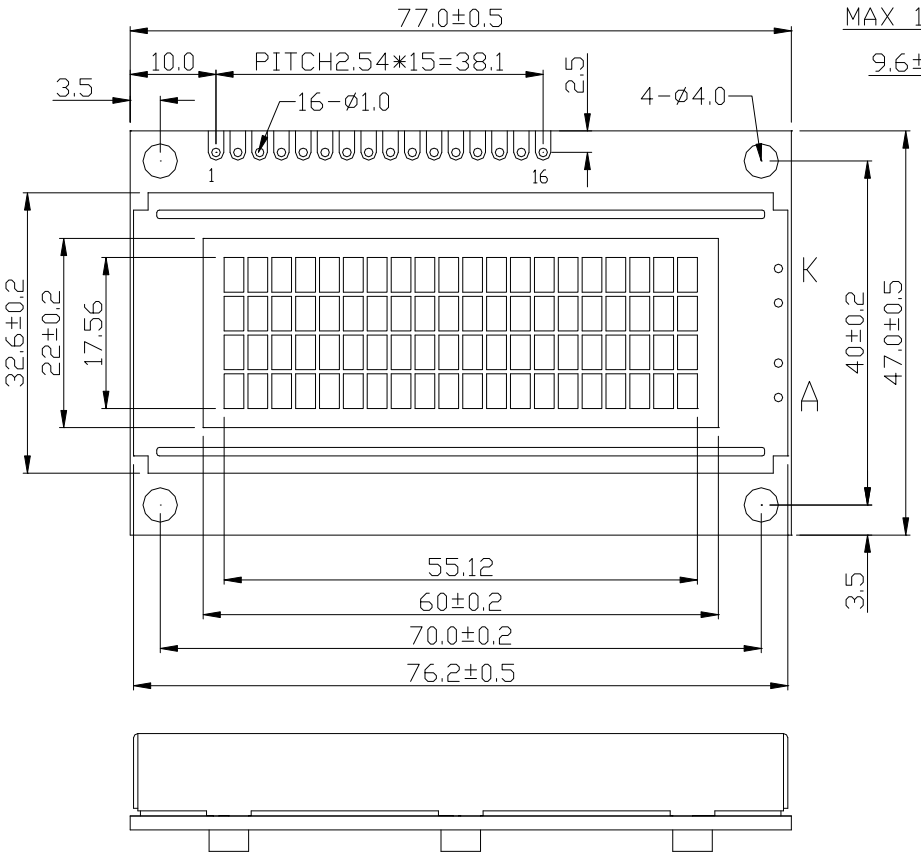
General Information Items	Specification	Unit	Note
	Main Panel		
Viewing Area (VA)	60.0 (H) x 22.0 (V)	mm	--
LCD Type	STN Positive	--	--
Viewing Angle	6:00	O'Clock	--
Polarizer	Transflective	--	--
Backlight Type	LED	--	--
Backlight Color	White	--	--
LCD IC	ST7066U-0A	--	--
Character Height	4.03	mm	--
Operating Temperature	-20 to +70	°C	--
Storage Temperature	-30 to +80	°C	--

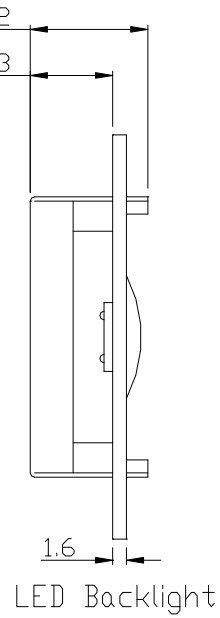
Mechanical Information

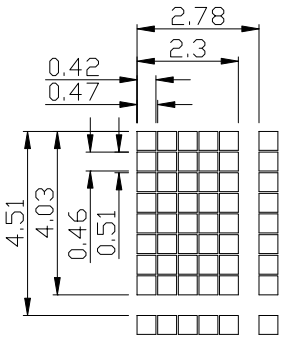
Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	--	77.0	--	mm	--
	Vertical (V)	--	47.0	--	mm	--
	Depth (D)	--	14.2	--	mm	--
Weight		--	45	--	g	Approximate

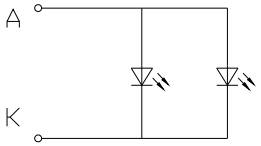
1. Outline Dimensions

Rev.	Description	Date
1.0	First	03/30/2023









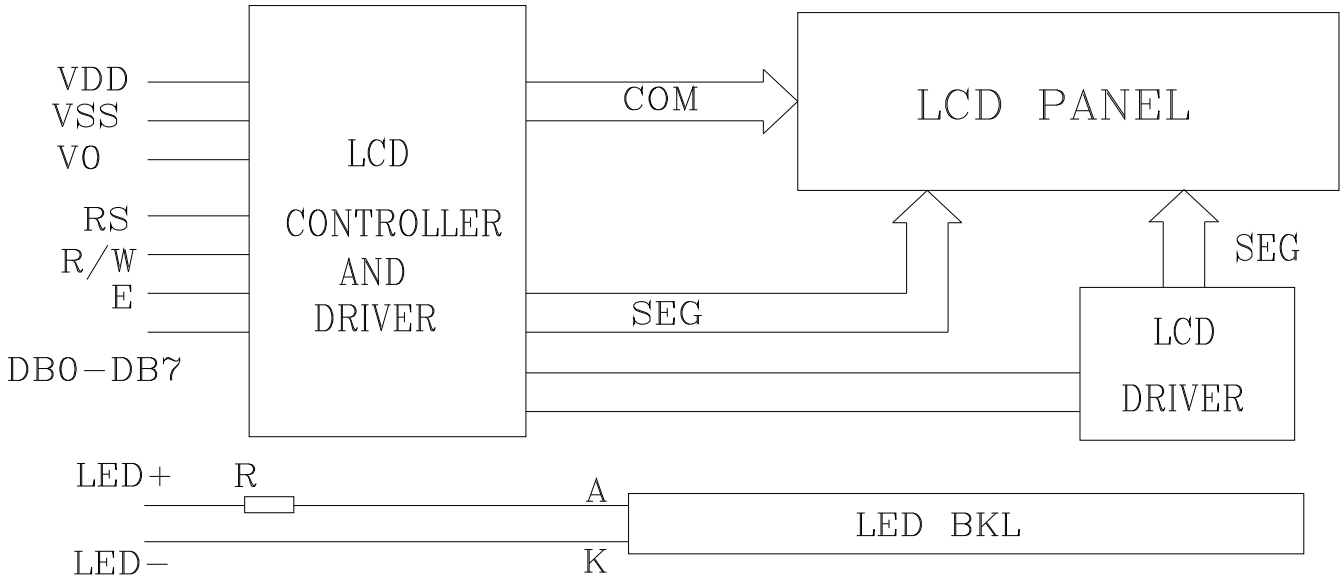
NO	PIN
1	VSS
2	VDD
3	V0
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	LED+
16	LED-

NOTES:

1. DISPLAY DRIVE: DUTY 1/16, BIAS 1/5, VLCD 4.5V, VDD 5.0V
2. DISPLAY MODE: STN GRAY, TRANSFLECTIVE, POSITIVE
3. LCM DRIVER IC: ST7066U-0A OR EQUIVALENT
4. OPERATING TEMPERATURE: -20°C TO +70°C
5. STORAGE TEMPERATURE: -30°C TO +80°C
6. VIEWING DIRECTION: 6:00
7. BACKLIGHT: SIDE WHITE
8. ROHS COMPLIANT

Model Name: C204CXBSGSW6WT55XAA			
General Tol: ±0.2			
Approvals	Date	Drawing No.:	Scale:
DWN:			
CHK:		Size:	Unit: mm
APP:			Page: 1/1

2. Block Diagram



3. Absolute maximum ratings

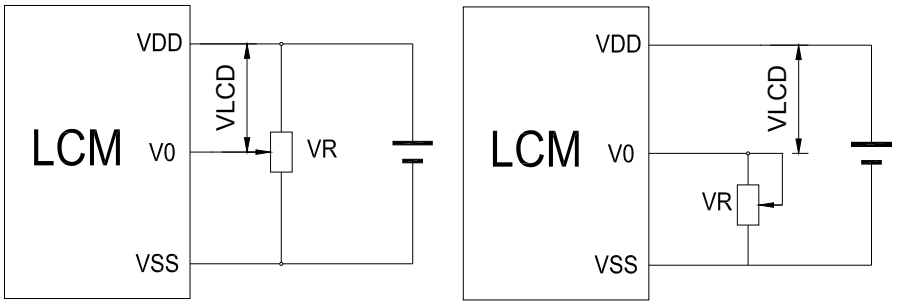
Item	Symbol	Min.	Max.	Unit
Power supply for Logic	VDD-VSS	-0.3	6.5	V
Power supply for LCD	VDD-V0	3	7	V
Input voltage	VIN	-0.3	VDD	V
Supply current for LED backlight	I_{LED}		40	mA
Operating temperature range	Top	-20	+70	℃
Storage temperature range	Tst	-30	+80	

4. Interface pin description

Pin no.	Symbol	External connection	Function
1	VSS	Power supply	Signal ground for LCM (GND)
2	VDD		Power supply for logic (+5.0V) for LCM
3	V0		Contrast adjust
4	RS	MPU	Register select signal
5	R/W	MPU	Read/write select signal
6	E	MPU	Operation (data read/write) enable signal
7-10	DB0-DB3	MPU	Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCM. These four are not used during 4-bit operation.
11-14	DB4-DB7	MPU	Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU
15	LED+	LED BLK power supply	Power supply for BKL (+5.0V, 20mA)
16	LED-		Power supply for BKL (GND)

Contrast Adjust

For Single Source



VDD~V0: LCD Driving voltage VR: 10k~20k

5. Optical characteristics

STN type display module (Ta=25℃, VDD=5.0V)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle (6 0'clock)	-	θ1	Cr≥3	-	30	-	deg
		θ2		-	40	-	
		Φ1		-	35	-	deg
		Φ2		-	35	-	
Contrast ratio		CR	-	-	10	-	-
Response time	Rise	tr		-	200	250	ms
	Fall	tf		-	300	350	

6. LED ratings

Item	Symbol	Min.	Typ.	Max.	Unit
Forward Voltage	VF	2.8	3.0	3.0	V
Forward current	If		20	30	mA
Power	P			0.2	W
Peak wave length	λp		-		nm
Luminance	Lv		60		Cd/m2

7. Electrical characteristics

DC characteristics

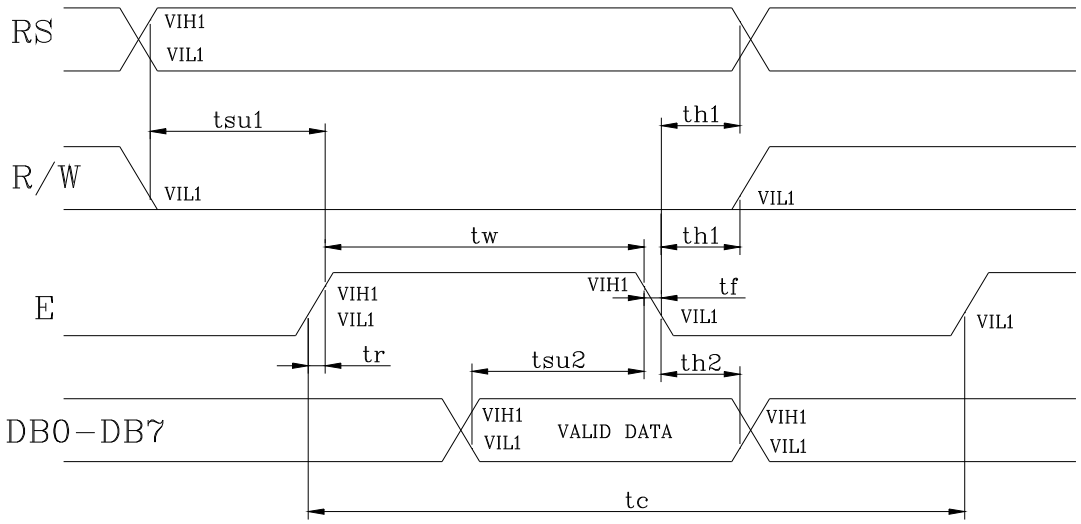
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage for LCD	VLCD	Ta=25℃	-	4.5	-	V
Input voltage	VDD		4.8	5.0	5.3	
Supply current	IDD	Ta=25℃, VDD=5.0V	-	1.5	2.0	mA
Input leakage current	ILKG		-	-	1.0	uA
"H" level input voltage	VIH		0.7 VDD	-	VDD	V
"L" level input voltage	VIL	Twice initial value or less	-0.3	-	0.6	
"H" level output voltage	VOH	LOH=-0.25mA	0.75 VDD	-	-	
"L" level output voltage	VOL	LOH=1.6mA	-	-	0.2 VDD	
Backlight supply voltage	VF		-	3.0	2.0	
Backlight supply current	IF	VDD=5.0V R=100Ω	-	20	-	uA

8. Write cycle

(Ta=25℃, VDD=5.0V)

Parameter	Symbol	Test pin	Min.	Typ.	Max.	Unit
Enable cycle time	TC	E	1200	-	-	ns
Enable pulse width	TW		450	-	-	
Enable rise/fall time	TR, TF		-	-	25	
RS; R/W setup time	TSU1	RS; R/W	60	-	-	
RS; R/W address hold time	TH1	RS; R/W	20	-	-	
Data output delay	TSU2	DB0~DB7	195	-	-	
Data hold time	TH2		10	-	-	

Write mode timing diagram

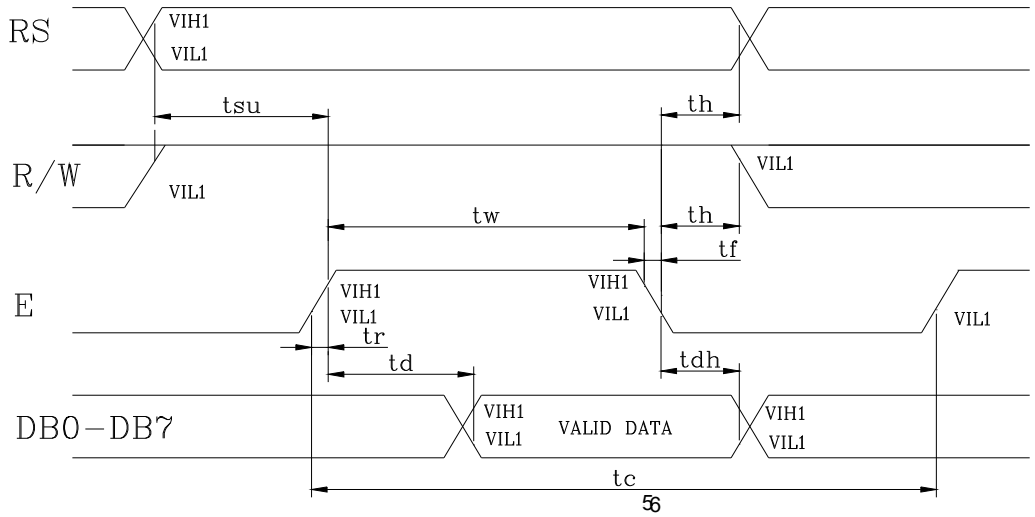


9. Read cycle

(Ta=25℃, VDD=5.0V)

Parameter	Symbol	Test pin	Min.	Typ.	Max.	Unit
Enable cycle time	TC	E	1200	-	-	ns
Enable pulse width	TW		450	-	-	
Enable rise/fall time	TR, TF		-	-	25	
RS; R/W setup time	TSU	RS; R/W	60	-	-	
RS; R/W address hold time	TH	RS; R/W	20	-	-	
Data output delay	TD	DB0~DB7	-	-	360	
Data hold time	TDH		20	-	-	

Read mode timing diagram



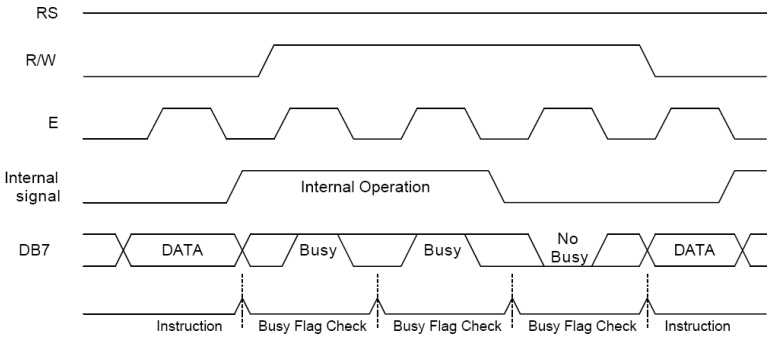
10. FUNCTION DESCRIPTION

System Interface

This chip has all two kinds of interface type with MPU : 4-bit bus and 8-bit bus. 4-bit bus and 8-bit bus is selected by DL bit in the instruction register.

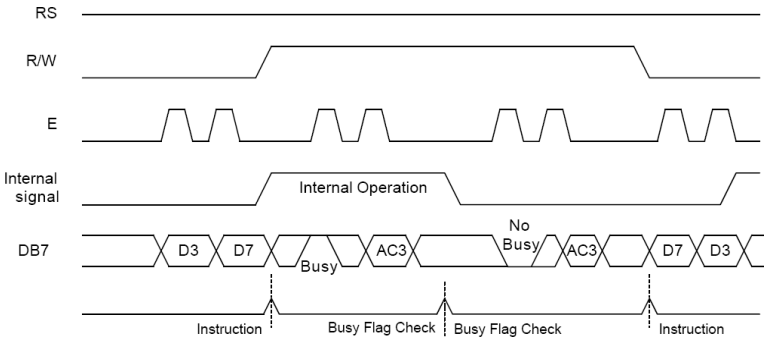
Interface with 8-bit MPU

When interfacing data length is 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7. Example of timing sequence is shown below.



Interface with 4-bit MPU

When interfacing data length is 4-bit, only 4 ports, from DB4 to DB7, are used as data bus. At first higher 4-bit (in case of 8-bit bus mode, the contents of DB4 - DB7) are transferred, and then lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed by two times. Busy Flag outputs "High" after the second transfer are ended. Example of timing sequence is shown below.



Busy Flag (BF)

When BF = "High", it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read, when RS = Low and R/W = High (Read Instruction Operation), through DB7 port. Before executing the next instruction, be sure that BF is not high.

Address Counter (AC)

Address Counter (AC) stores DDRAM/CGRAM address, transferred from IR. After writing into (reading from) DDRAM/CGRAM, AC is automatically increased (decreased) by 1. When RS = "Low" and R/W = "High", AC can be read through DB0 - DB6 ports.

Display Data RAM (DDRAM)

DDRAM stores display data of maximum 80 x 8 bits (80 characters). DDRAM address is set in the address counter (AC) as a hexadecimal number.

Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
DDRAM address	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53
	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67

CGROM (Character Generator ROM)

CGROM has a 5 x 8 dots 204 characters pattern and a 5 x 10 dots 32 characters pattern. CGROM has 204 character patterns of 5 x 8 dots.

CGRAM (Character Generator RAM)

CGRAM has up to 5 8 dot, 8 characters. By writing font data to CGRAM, user defined characters can be used.

Character Code (DDRAM Data)									CGRAM Address						Character Patterns (CGRAM Data)							
b8	b7	b6	b5	b4	b3	b2	b1	b0	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	-	0	0	0	0	0	0	0	0	0	-	-	-	1	1	1	1	1
						0	0	0				0	0	1				0	0	1	0	0
						0	0	0				0	1	0				0	0	1	0	0
						0	0	0				0	1	1				0	0	1	0	0
						0	0	0				1	0	0				0	0	1	0	0
						0	0	0				1	0	1				0	0	1	0	0
						0	0	0				1	1	0				0	0	1	0	0
						0	0	0				1	1	1				0	0	0	0	0
0	0	0	0	0	-	0	0	1	0	0	1	0	0	0	-	-	-	1	1	1	1	0
						0	0	1				0	0	1				1	0	0	0	1
						0	0	1				0	1	0				1	0	0	0	1
						0	0	1				0	1	1				1	1	1	1	0
						0	0	1				1	0	0				1	0	1	0	0
						0	0	1				1	0	1				1	0	0	1	0
						0	0	1				1	1	0				1	0	0	0	1
						0	0	1				1	1	1				0	0	0	0	0

Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns (CGRAM Data)

Notes:

1. Character code bits 0 to 2 correspond to CGRAM address bits 3 to 5 (3 bits: 8 types).
2. CGRAM address bits 0 to 2 designate the character pattern line position. The 8th line is the cursor position and its display is formed by a logical OR with the cursor. Maintain the 8th line data, corresponding to the cursor display position, at 0 as the cursor display. If the 8th line data is 1, 1 bit will light up the 8th line regardless of the cursor presence.
3. Character pattern row positions correspond to CGRAM data bits 0 to 4 (bit 4 being at the left).
4. As shown Table, CGRAM character patterns are selected when character code bits 4 to 7 are all 0. However, since character code bit 3 has no effect, the R display example above can be selected by either character code 00H or 08H.
5. 1 for CGRAM data corresponds to display selection and 0 to non-selection. “-“: Indicates no effect.

Cursor/Blink Control Circuit

It controls cursor/blink ON/OFF at cursor position.

11. Instruction description

11.1. Outline

To overcome the speed difference between the internal clock of ST7066U and the MPU clock, ST7066U performs internal operations by storing control in formations to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus (Refer to Table7). Instructions can be divided largely into four groups:

1) ST7066U function set instructions (set display methods, set data length, etc.)
2) Address set instructions to internal RAM
3) Data transfer instructions with internal RAM
4) Others

The address of the internal RAM is automatically increased or decreased by 1.

Note: during internal operation, busy flag (DB7) is read “High”.
Busy flag check must be preceded by the next instruction.

11.2. Instruction Table

Instruction	Instruction code										Description	Execution time (fosc= 270 KHZ)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write “20H” to DDRA and set DDRAM address to “00H” from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to “00H” From AC and return cursor to Its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction And blinking of entire display	39us
Display ON/ OFF control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and Blinking of cursor (B) on/off Control bit.	
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display Shift control bit, and the Direction, without changing of DDRAM data.	39us
Function set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-Bit/4-bit), numbers of display Line (N: =2-line/1-line) and, Display font type (F: 5x11/5x8)	39us
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address. Counter.	39us
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address. Counter.	39us

Read busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal Operation or not can be known By reading BF. The contents of Address counter can also be read.	0us
Write data to Address	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43us
Read data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43us

NOTE:

When an MPU program with checking the busy flag (DB7) is made, it must be necessary 1/2fosc is necessary for executing the next instruction by the falling edge of the “E” signal after the busy flag (DB7) goes to “Low”.

11.3. Contents

1) Clear display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H” (space code) to all DDRAM address, and set DDRAM address to “00H” into AC (address counter).

Return cursor to the original status, namely, bring the cursor to the left edge on the fist line of the display.

Make the entry mode increment (I/D=“High”).

2) Return home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Return home is cursor return home instruction.

Set DDRAM address to “00H” into the address counter.

Return cursor to its original site and return display to its original status, if shifted.

Contents of DDRAM does not change.

3) Entry mode set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D: increment / decrement of DDRAM address (cursor or blink)

When I/D=“high”, cursor/blink moves to right and DDRAM address is increased by 1.

When I/D=“Low”, cursor/blink moves to left and DDRAM address is increased by 1.

*CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.

SH: shift of entire display

When DDRAM read (CGRAM read/write) operation or SH=“Low”, shifting of entire display is not performed. If SH =“High” and DDRAM write operation, shift of entire display is performed according to I/D value. (I/D=“high”. shift left, I/D=“Low”. Shift right).

4) Display ON/OFF control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit

When D=“High”, entire display is turned on.

When D=“Low”, display is turned off, but display data remains in DDRAM.

C: cursor ON/OFF control bit

When D=“High”, cursor is turned on.

When D=“Low”, cursor is disappeared in current display, but I/D register preserves its data.

B: Cursor blink ON/OFF control bit

When B=“High”, cursor blink is on, which performs alternately between all the “High” data and display characters at the cursor position.

When B=“Low”, blink is off.

5) Cursor or display shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifting of right/left cursor position or display without writing or reading of display data. This instruction is used to correct or search display data.
During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line.
Note that display shift is performed simultaneously in all the lines.
When display data is shifted repeatedly, each line is shifted individually.
When display shift is performed, the contents of the address counter are not changed.
Shift patterns according to S/C and R/L bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6) Function set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL: Interface data length control bit
When DL="High", it means 8-bit bus mode with MPU.
When DL="Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode. When 4-but bus mode, it needs to transfer 4-bit data twice.

N: Display line number control bit
When N="Low", 1-line display mode is set.
When N="High", 2-line display mode is set.

F: Display line number control bit
When F="Low", 5x8 dots format display mode is set.
When F="High", 5x11 dots format display mode.

7) Set CGRAM address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.
The instruction makes CGRAM data available from MPU.

8) Set DDRAM address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.
This instruction makes DDRAM data available form MPU.
When 1-line display mode (N=LOW), DDRAM address is form "00H" to "4FH".In 2-line display mode (N=High), DDRAM address in the 1st line form "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

9) Read busy flag & address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether ST7066U is in internal operation or not.
If the resultant BF is "High", internal operation is in progress and should wait BF is to be LOW, which by then the nest instruction can be performed. In this instruction you can also read the value of the address counter.

10) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.
The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DDRAM address set, CGRAM address set).
RAM set instruction can also determine the AC direction to RAM.
After write operation. The address is automatically increased/decreased by 1, according to the entry mode.

11) Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not yet determined. If RAM data is read several times without RAM address instructions set before, read operation, the correct RAM data can be obtained from the second. But the first data would be incorrect, as there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction, it also transfers RAM data to output data register.

After read operation, address counter is automatically increased/decreased by 1 according to the entry mode.

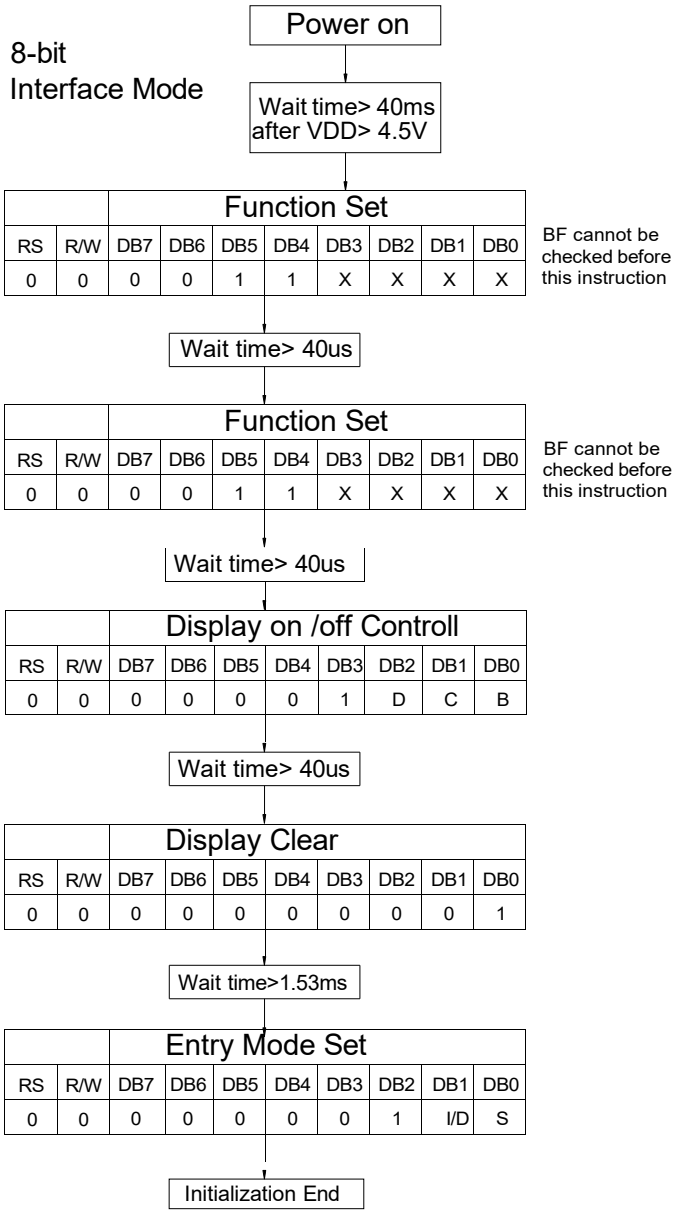
After CGRAM read operation, display shift may not be executed correctly.

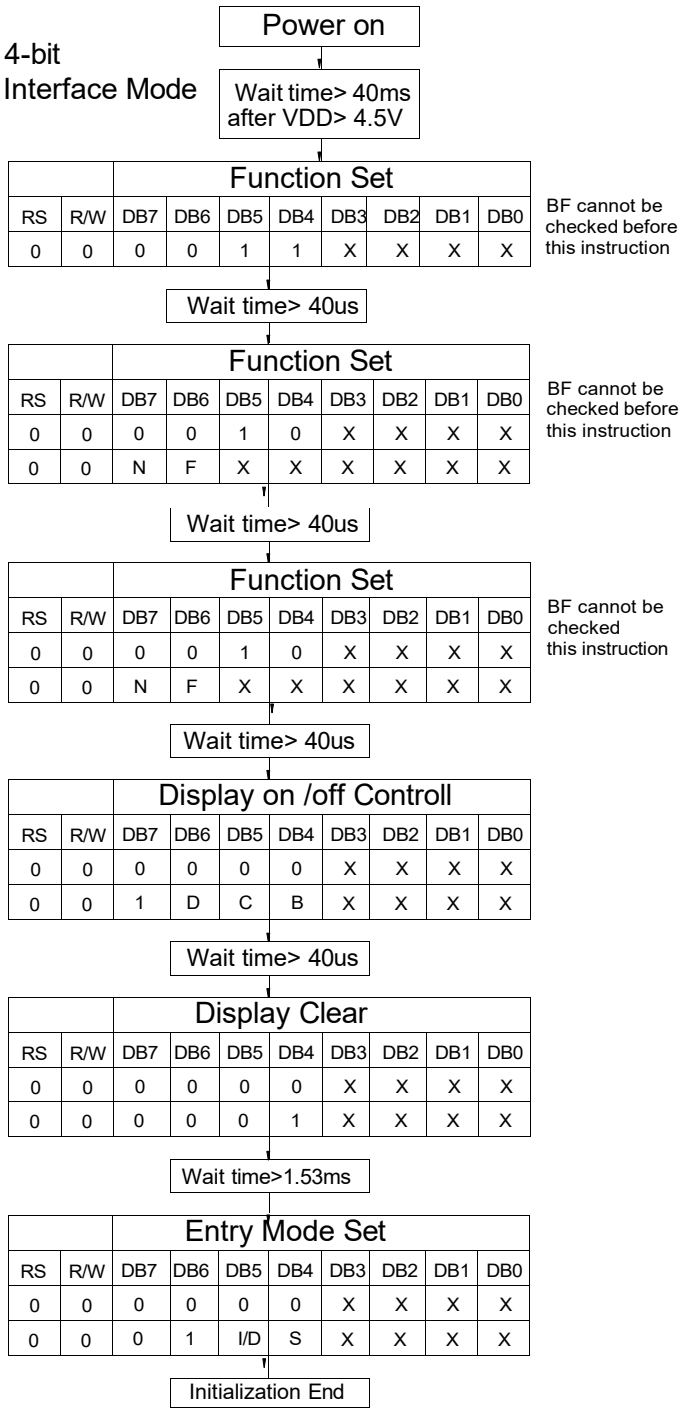
NOTE: In case of RAM write operation, AC is increased/decreased by 1 as in read operation.
At this time, AC indicates next address position, but only the previous data can be read by the read instruction.

12. Standard character pattern

Upper 4bit / Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															

13. Initializing By Instruction





14. Cautions and Handling

General Precautions:

1. LCD panel is made of glass. Avoid excessive mechanical shock or applying strong pressure onto the surface of display area.
2. The polarizer used on the display surface is easily scratched and damaged. Extreme care should be taken when handling. To clean dust or dirt off the display surface, wipe gently with cotton, or other soft material soaked with isoproply alcohol, ethyl alcohol or trichlorotriflorothan. Do not use water, ketone or aromatics and never scrub hard.
3. Do not tamper in any way with the tabs on the metal frame.
4. Do not make any modification on the PCB without consulting.
5. When mounting the LCM, make sure that the PCB is not under any stress such as bending or twisting. Elastomer contacts are very delicate and missing pixels could result from slight dislocation of any of the elements.
6. Avoid pressing on the metal bezel, otherwise the elastomer connector could be deformed and lose contact, resulting in missing pixels and cause rainbow on the display.
7. Be careful not to touch or swallow liquid crystal that might leak from a damaged cell. Any liquid crystal adheres to skin or clothes, wash it off immediately with soap and water.

Static Electricity Precautions:

1. CMOS-LSI is used for the module circuit; therefore, operators should be grounded whenever he/she comes into contact with the module.
2. Do not touch any of the conductive parts such as the LSI pads, the copper leads on the PCB and the interface terminals with any parts of the human body.
3. Do not touch the connection terminals of the display with bare hand; it will cause disconnection or defective insulation of terminals.
4. The modules should be kept in anti-static bags or other containers resistant to static for storage.
5. Only properly grounded soldering irons should be used.
6. If an electric screwdriver is used, it should be grounded and shielded to prevent sparks.
7. The normal static prevention measures should be observed for work clothes and working benches.
8. Since dry air is inductive to static, a relative humidity of 50-60% is recommended.

Soldering Precautions:

1. Soldering should be performed only on the I/O terminals.
2. Use soldering irons with proper grounding and no leakage.
3. Soldering temperature: 280°C+10°C
4. Soldering time: 3 to 4 second.
5. Use eutectic solder with resin flux filling.
6. If flux is used, the LCD surface should be protected to avoid spattering flux.
7. Flux residue should be removed.

Operation Precautions:

1. The viewing angle can be adjusted by varying the LCD driving voltage Vo.
2. Since applied DC voltage causes electro-chemical reactions, which deteriorate the display, the applied pulse waveform should be a symmetric waveform such that no DC component remains. Be sure to use the specified operating voltage.
3. Driving voltage should be kept within specified range; excess voltage will shorten display life.
4. Response time increases with decrease in temperature.
5. Display color may be affected at temperatures above its operational range.
6. Keep the temperature within the specified range usage and storage. Excessive temperature and humidity could cause polarization degradation, polarizer peel-off or generate bubbles.
7. For long-term storage under 40C is required and the relative humidity should be kept below 60%.