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LCD Resources:
MIPI and LVDS Display Interfaces

The MIPI and LVDS Display Interfaces

Two common high-speed communication protocols for displays are MIPI DSI and LVDS. The Mobile Industry Processor Interface, also known as MIPI, is a high-speed differential protocol that is commonly used in cellphones. Specifically, the MIPI Display Serial Interface (DSI) technology is designed for display communication. LVDS is a technique that uses differential signaling at low voltages to transmit display data. While LVDS is a broad technical specification for signaling, it has become synonymous in the display industry with the FPD-Link protocol (Flat Panel Display Link). MIPI DSI and FPD-Link are both communication protocols that use LVDS as their standard.

These communication protocols send display data through differential signaling which makes the transmission of data faster and require fewer data lines. These interfaces are good options for large displays, high graphics definition and fast frame rates. Because these signals are sent through a differential sequence over bidirectional data lanes, fewer connections are required to interface with the display.

The MIPI Interface

The MIPI DSI was designed to interface display's for cellphones and smart devices and is the most common connection interface for these devices today. This interface uses LVDS signaling over a D-PHY layer to communicate with the display over two or four data pairs. In addition to the data lines, the MIPI interface has a differential clock pair that times the signals at a high frequency.

These clock and data lanes are triggered at low voltages which make these displays low powered. Because this interface can signal data at a very high speed, a large amount of data can be sent over the minimum frame rate requirements. This means that MIPI interface displays can be high resolution, render high color, and can be used for high-speed applications such as video transmission. Below is an example of a Focus LCDs MIPI interfaced display, [E43RB-FW405-C](#). This display is a 4.3" TFT with 480x800 pixels and is connected through a 2-lane MIPI interface. Additional features of this display are reviewed below.



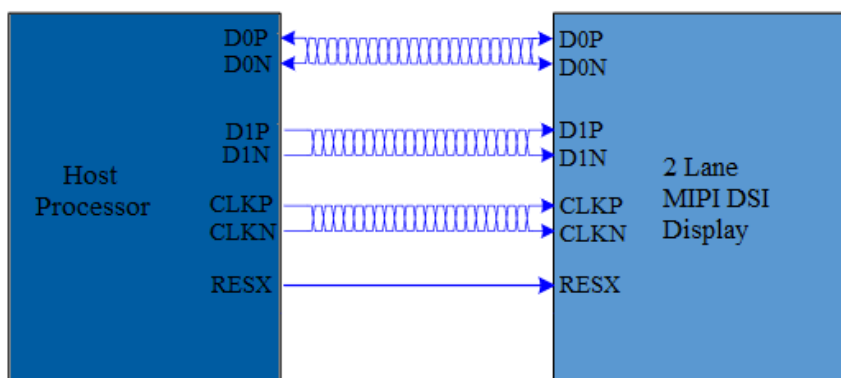
Characteristics	Specification	Unit
Size	62.50(H) x 105.55 (V) (4.3 inch)	mm
Display Colors	16.7M	colors
Resolution	480(RGB)x800	pixels
Interface	2-lane MIPI	-
Touch Interface	Capacitive	-
Input Voltage	3.3	V
Brightness	405	nits
Operating temperature	-20~+70	°C
Storage temperature	-30~+80	°C

The controller for this display is a TFT driver embedded in the display and is signaled over the 2-lane MIPI interface. This IC is the ILI9806 single chip driver without internal GRAM. This is important to note because RAM will need to be provided externally for the displays frame buffer. The connection ports to the embedded display controller are through a 20-pin ribbon cable that will be used to program the display. Below are the pin connections for this 2-lane MIPI interfaced display.

NO.	Symbol	Description	I/O
1	NC	--	--
2	LEDK	Cathode pin of the backlight	P
3	NC	--	--
4	LEDA	Anode pin of the backlight	P
5	NC	--	--
6	VCI	Supply voltage (3.3V)	P
7	IOVCC	I/O power supply (1.8-3.3V)	P
8	TE	Tearing effect output signal.	O
9	RESET	External reset signal of the device. Initializes the chip.	I
10	GND	Ground	P
11	D1P	MIPI DSI differential data pair, lane 2. (DSI-Dn+/-)	I/O
12	D1N		
13	GND	Ground	P
14	CLKP	MIPI DSI differential clock pair (DSI-Dn+/-)	I/O
15	CLKN		
16	GND	Ground	P
17	D0P	MIPI DSI differential data pair, lane 1. (DSI-Dn+/-)	I/O
18	D0N		
19	GND	Ground	P
20	GND	Ground	P

I:Input, O:Output, P:Power

This two lane MIPI DSI interface transmits signals through differential pairs so that each lane has two differential pins. The range of data transmission of the MIPI D-PHY layer is 8Mbps-2.5Gbps. There are two modes that the MIPI DSI interface sends signals in. One is for sending commands to the registers in the frame buffer to initialize the display. The other is a high-speed video mode that transmits data in real time. The low power mode has a larger voltage swing and should be used for controlling the system, such as sending or reading commands. The high-speed signals have a low voltage swing as should be used for data traffic such as transmitting video.



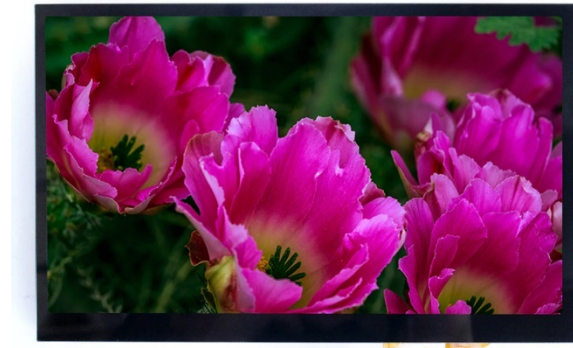
Because of the high-speed data transmission, the external processor used in the applications with a MIPI interfaced display must possess the minimum attributes required by this interface. Considerations should be made such as oscillator frequency, location and size of RAM, and EMI of other devices. The MIPI interface has very low EMI due to the low voltage of the differential signaling and the equal and opposite data pairs. EMI of radio frequencies should be monitored to prevent noise on the high-speed signals over longer distances.

While microcontrollers with MIPI DSI interfaces are not predominant in the industry, graphics controllers can be implemented to support a processor with the demands of a MIPI interface. MIPI interface displays are beneficial for rendering high color and high-definition images. Higher color requires more data to be sent for each pixel and a higher resolution means more pixels. This results in a large amount of data which needs a location in memory for the minimum frame buffer in order to maintain an image.

Often times the display's embedded IC will provide internal GRAM sufficient for the frame buffer but this should be verified with each display in the specification sheet of the IC. Graphics controllers often provide the memory and oscillator requirements to support these high-performance displays.

The LVDS Interface

The Flat Panel Display Link interface (FPD-Link) has become synonymous with the LVDS interface in the display industry. The LVDS interface explained in this note will be in reference to the FPD-Link protocol. This protocol was the original high speed display interface that uses differential signaling at very low voltages to transmit data at a high frequency. This interface is most commonly used for connecting laptops and televisions to their graphics controllers. The LVDS interface transmits data over four differential data pairs six or eight bits at a time.

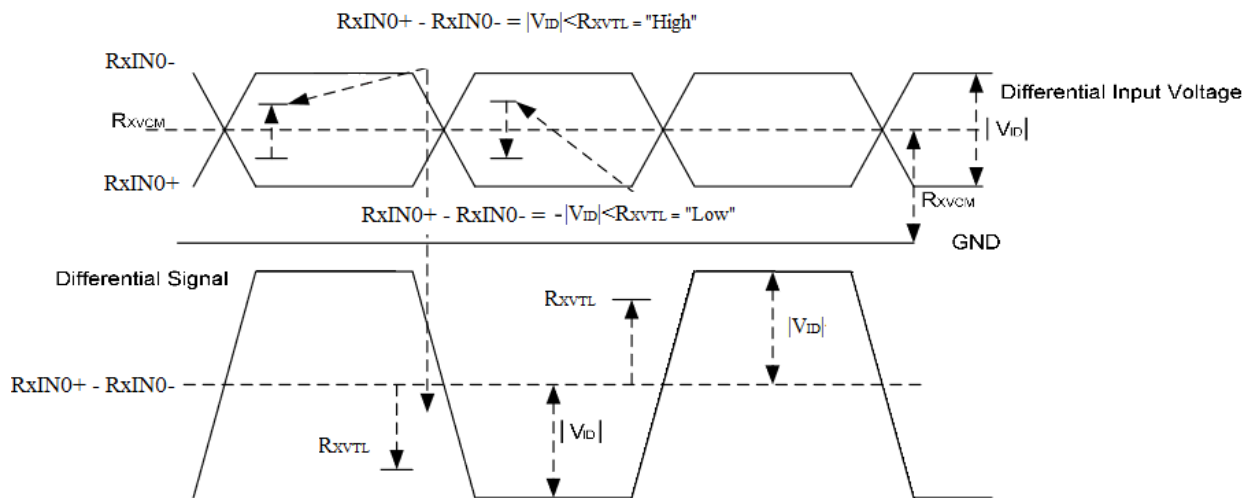


One example of a display that is connected through an LVDS interface is [E70RA-HW520-C](#). This display is a 7.0" TFT with 1024x600 pixels and can display up to 16.7M colors. This display has embedded gate and a source driver IC's that can be programmed from a standard graphics controller. Below are additional features of this LVDS display.

Characteristics	Specification	Unit
Size	154.21(H) x 85.92 (V) (7.0 inch)	mm
Display Colors	16.7M	colors
Resolution	1024(RGB)x600	pixels
Interface	6/8-bit LVDS	-
Touch Interface	Capacitive	-
Input Voltage	3.3	V
Brightness	520	nits
Operating temperature	-20~+70	°C
Storage temperature	-30~+80	°C

The display communicates over an LVDS interface to an attached HDMI module, which supports the gate and driver signaling as well as the capacitive touch interface. The LVDS interface of this display accepts RGB data in sequences of six or eight bits corresponding to the 16-bit, 18-bit and 24-bit color depths. This display has four differential data pairs and one differential clock pair.

Similar to the MIPI DSI interface, this protocol is low voltage and uses differential signaling. Additionally, this interface has low EMI noise and has a high frequency. This display operates at a clock frequency of 65MHz for the LVDS interface. The clock frequency is determined by the interface capabilities and the resolution of the display in order to maintain a refresh rate of 60Hz.



Below is a description of each of the pins that you can find on an LVDS interface display. This is a typical pin configuration for an LVDS interface display. It is important to verify that the pin connection matches with the graphics controller before connection because some LVDS displays may have alternative pin mappings and features.

NO.	Symbol	Description	I/O
1	NC	--	--
2-3	VDD	Supply Voltage (3.3V)	P
4	NC	--	--
5	RESET	Reset signal of the device.	I
6	STBYB	Standby mode of the device.	I
7	GND	Ground	P
8	RXIN0-	Differential data pair 1 for the LVDS interface	I/O
9	RXIN0+		
10	GND	Ground	P
11	RXIN1-	Differential data pair 2 for the LVDS interface	I/O
12	RXIN1+		
13	GND	Ground	P
14	RXIN2-	Differential data pair lane 3 for the LVDS interface	I/O

15	RXIN2+		
16	GND	Ground	P
17	RXCLKN-	Differential clock pair for the LVDS interface	I
18	RXCLKN+		
19	GND	Ground	P
20	RXIN3-	Differential data pair lane 4 for the LVDS interface.	I/O
21	RXIN3+		
22	GND	Ground	P
23-24	NC	--	--
25	GND	Ground	P
26	NC	--	--
27	DIMO	Backlight dimming signal for backlight	O
28	SELB	LVDS data format selection. 6-bit or 8-bit LVDS interface	I
29	NC	--	--
30	GND	Ground	P
31-32	LEDK	Cathode pin of the backlight	P
33	L/R	Horizontal shift direction (source output)	I
34	U/D	Vertical shift direction (gate output)	I
35-38	NC	--	--
39-40	LEDA	Anode pin of the backlight	P

I: Input, O: Output, P: Power

The LVDS interface for displays reduces the pin count of the RGB signals to a few differential pairs. This is beneficial for hardware connection while still maintaining the large amount of data transmitted. The differential signaling also reduces EMI noise because the signals are equal and opposite and cancel out electromagnetic radiation effects. Another benefit for LVDS displays is the standard pinout for the connection cable. This makes these displays accessible to many graphic controllers and predesigned systems.

Considerations

The high-speed differential interfaces provide capabilities for high performance displays. High performance features such as high color and high resolution require more data to be transmitted per pixel on the display. This requires a larger amount of memory to be provided by the system. In addition to memory, the minimum clocking requirements of these high-speed interfaces will require a higher frequency oscillator. This will require a more advanced controller or an additional graphics controller to communicate with these displays.

As technology advances with display communication interfaces, so do the methods of reducing the complexity of the system. MIPI DSI and LVDS have collaborated with VESA (Video Electronics Standards Association) to integrate video compression with their interfaces, which reduces the memory constraint of the display. The display technology itself is low cost, power efficient and high performing. The devices used to communicate with these displays are making progress on reducing cost and increasing availability over time.

These differential display interfaces are great options for applications where the display is an integral component of the product as opposed to a peripheral device to the system. This is why they are featured in smart devices, such as cellphones, laptops, and televisions, where the core application is through the display. It has become increasingly common to replace analog interfaces with digital, such as replacing a push button with a capacitive touch display. This makes these differential interfaces the new standard for display communication.