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Application Note FAN4218

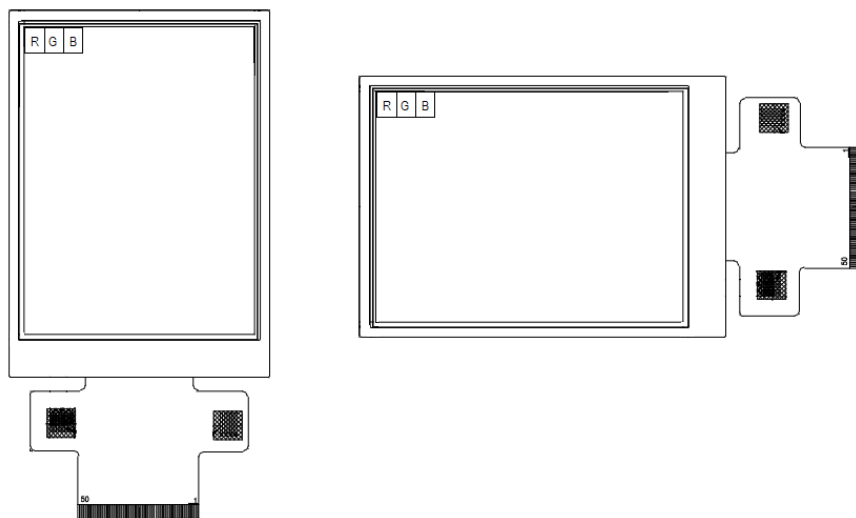
Landscape and Portrait Mode for TFTs

This application note will discuss switching between landscape and portrait modes on TFT displays.

Landscape and Portrait Modes for TFT Displays

This note will discuss how to switch between the landscape and portrait orientations of a TFT display. The landscape mode refers to the horizontal display orientation and the portrait mode refers to the vertical orientation of the pixel data.

Having the ability to switch display orientations can provide more options for the display's application. The display orientation adjustments can also provide an option to switch orientation based on the direction the user is viewing it from. This application is seen in cellphone and table displays. This note will elaborate on each orientation and the software requirements of switching between the two.



The display orientation is set through software commands to the on-chip display control registers. These commands are consistent across the different display drivers. The commands should be confirmed in the datasheet for each display. The landscape and portrait modes will define the horizontal and vertical settings of the resolution.

Each of these modes defines how the pixel data is framed on the display. This means that the horizontal and vertical resolutions are switched. The pixel data can be switched from top to bottom, bottom to top, left to right and right to left. This means that the display can be viewed correctly from any rotational direction.



The display used in this application is Focus LCDs part number: [E32RA-CW380-N](#). This is a 3.2-inch TFT with a 240 x 320 pixel resolution. This display supports vertical and horizontal pixel orientations that can be chosen based on the application. The viewing angle of this display is in the 6 o'clock direction.

This display also offers a variety of driving options and connection interfaces. This makes the display customizable for a range of applications. The display's interface can be chosen based on available resources and desired function. Additional features of this display are reviewed in the table below.

Description	Specification	Unit	Note
Display Area	48.06 x 64.80	mm ²	3.2"
Driver Element	TFT Active Matrix	--	--
Display Colors	65k/252k	colors	Programmable
Resolution	240 x 320	pixels	
Viewing Angle	6:00	o'clock	Bottom
Interfaces	Serial, MCU, RGB	--	--
Display Mode	Transmissive	--	White
Controller IC	ST7789V	--	--
Pixel Arrangement	RGB Vertical Stripe	--	--

Display Pin Location

The display is connected through a 50 pin FPC cable which provides access to the internal display controller IC, ST7789V. The details of this chip on glass (COG) embedded display driver are detailed in the

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[datasheet](#) of the device. The interface chosen for this application is the 3-wire Serial interface that requires the fewest number of interface pins to connect.

This application will demonstrate how to communicate the commands required to switch between vertical and horizontal display modes. This is done through 8-bit data blocks that are sent to the control registers. The 3-wire serial interface will be sufficient for this demonstration.

The pins available on this display are described in the table below.

No.	Symbol	Description	I/O
1	GND	Ground	P
2-5	NC	Resistive Touch panel control pins. Not connected.	--
6-7	IOVCC	Supply voltage for I/O (1.8-3.3V)	P
8-9	VCI	Supply voltage for power circuits (3.3V)	P
10	IM2	Interface selection pins.	I
11	IM1		I
12	IM0		I
13	RESET	Reset signal of the device	I
14	CS	Chip select signal	I
15	D/CX (SPI_SCL)	Data and command pin for the parallel interface. Serial clock for the 3 and 4 wire SPI interfaces.	I
16	WR (SPI_RS)	Write signal for the parallel interface. Register select signal for the 4-wire SPI interface.	I
17	RD	Read signal for the parallel interface.	O
18	VSYNC	Vertical synchronization signal for the RGB parallel interface.	I
19	HSYNC	Horizontal synchronization signal for the RGB parallel interface.	I
20	ENABLE	Enable signal for the RGB parallel interface.	I
21	DOTCLK	Pixel (dot) clock signal for the RGB parallel interface.	I
22	SDA	Serial data input and output in for the 3-wire and 4-wire serial interface	I/O
23-40	DB[0:17]	Parallel data bus for the RGB and MCU parallel interfaces	I/O
41	SDO	Serial data output pin for the 4-wire SPI interface	O
42	GND	Ground	P
43	LEDA	Anode pin of the backlight	P
44-49	LEDK1-LEDK6	Cathode pins of the backlight	P
50	GND	Ground	P

I: Input, O: Output, P: Power

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Interface Selection

The interface is selected through the hardware pins 10, 11 and 12 which are indicated in the previous table. These pins specify which interface is being used before sending any data to the control registers. The interface selection pins can be set to high or low to select the interface.

Below are the interface selection pin options for IM2, IM1 and IM0 and the corresponding interface and pin requirements. The RGB parallel interface is selected when the interface pins are set to either serial interface selection.

Interface Selection Table

IM2	IM1	IM0	Interface	Pins Required	Notes
0	0	0	16-bit parallel MCU	DB17-DB10, DB8-DB1	8080, 6800
0	0	1	8-bit parallel MCU	DB17-DB10	8080, 6800
0	1	0	18-bit parallel MCU	DB17-DB0	8080, 6800
0	1	1	9-bit parallel MCU	DB17-DB9	8080, 6800
1	0	1	3-wire Serial	SDA SCL CS	9-bit
1	1	0	4-wire Serial	SDA SCL CS RS	8-bit

The RGB parallel interface is selected for either serial interface. The RGB parallel interface can communicate over 16 or 18 data buses. The required pins for the RGB parallel interface are described in the table below.

RGB Interface Selection Table

IM2	IM1	IM0	Interface		Pins Required	Notes
1	0	1	RGB	16-bit RGB	DB17-DB13, DB11-DB6, DB5-DB1	(565)
1	1	0		18-bit RGB	DB17-DB0	(666)

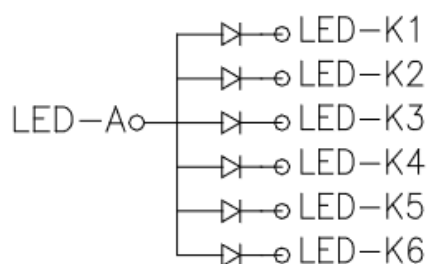
The interface used in this example is the 3-wire Serial interface which uses one data pin, one clock and one chip enable pin. This interface is selected by setting IM2, IM1 and IM0 = [1, 0, 1]. The unused interface pins can be set to ground, IOVCC, or remain unconnected.

The additional pins used for this application are the reset pin and the power pins. The reset pin is used to reset the IC to clear the previous initialized register settings. The power required for the digital communication is set at 1.8-3.3V.

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Backlight LED Circuit

The backlight is powered externally at a voltage of 3.2 V and 120 mA. The constant current method of driving the backlight is suggested for proper LED uniformity across the display. The backlight circuit for this display contains 6 LEDs in parallel.



The backlight is lit by six white LEDs that illuminate the back plane of the display. The brightness of the backlight is approximately 380 nits. The backlight is required to be on for the pixels to appear because the display is transmissive.

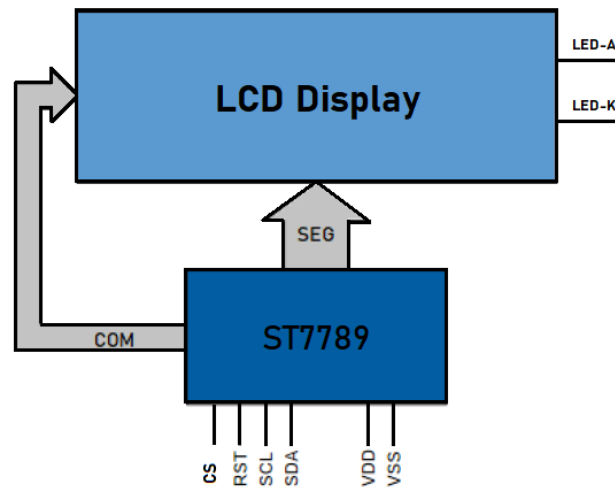
The anode pin of the backlight is supplied the positive voltage of 3.2V at 120mA indicated by the symbol LED-A in the circuit. The six cathode pins are labeled as the LED-K pins and should be connected to the voltage ground that corresponds to the voltage supplied at LED-A.

The backlight power can be supplied by a DC power supply or by a constant current LED driver. The LED driver should be able to support up to 6 LEDs in parallel at 3.2V and 120mA.

When the backlight and digital voltage is supplied to the display, the default screen should be white. This is what is meant by the display mode “Transmissive, normally white” in the description.

Interface Pin Connection

The 3-wire serial interface uses three data pins, a reset pin, and power pins. The serial interface requires the fewest number of pin connections to be connected to the display. The serial interface uses 9-bit command chunks to communicate the register command settings. Since the commands and interface require minimal data and connections, any microcontroller can be used.

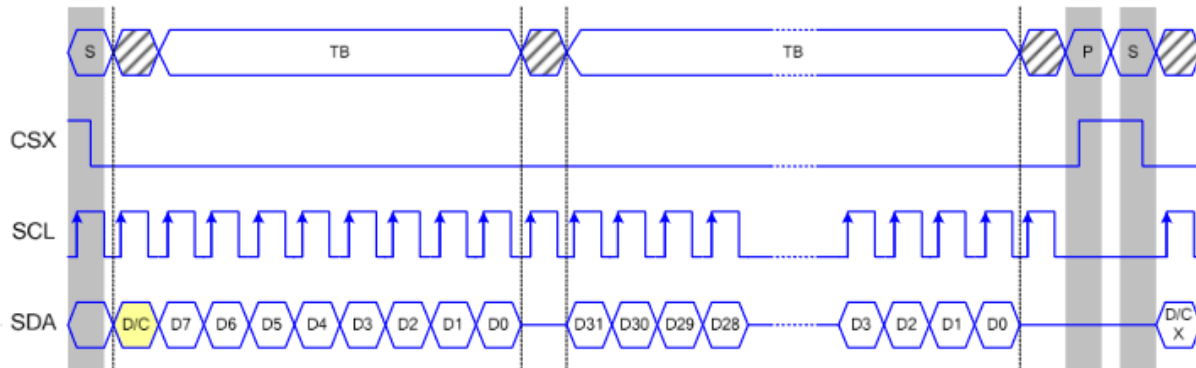


The pins required to operate the display with this interface are described in the table below.

No	Symbol	Description	Connection
1	GND	Ground	Digital Ground (GND)
6-7	IOVCC	Digital supply voltage	1.8V
8-9	VDD	Supply voltage	3.3V
10	IM2	Interface selection pins	1.8V
11	IM1		GND
12	IM0		1.8V
13	RESET	Reset signal	Reset pin
14	CS	Chip select	Digital pin 10
15	SCL	Serial clock	Digital pin 13
22	SDA	Serial data input & output	Digital pin 11
42	GND	Ground	GND
43	LEDA	Backlight anode	3.2 V external power
44-49	LEDK	Backlight cathode	Ground external power
50	GND	Ground	GND

Display Initialization Commands

The display must be initialized through the 8-bit commands over the 9-bit serial interface. The first bit of the 9-bit serial interface signal will indicate whether the following byte is received as a command instruction or a data instruction. The 3-wire serial interface uses one pin as the input and output data pin.



Below are the commands that initialize the display and the controller ST7789V with standard display settings. The orientation used in the following initialization is in the vertical mode. The color format used is the 16-bit (565) format. Each of these commands are explained in detail in the [datasheet](#) of the controller.

```

write_command(0xB2);    //PORCTRL
write_data(0x0C);
write_data(0x0C);
write_data(0x00);
write_data(0x33);
write_data(0x33);

write_command(0xB7);    //GCTRL
write_data(0x35);

write_command(0xBB);    //VCOM
write_data(0x30);

write_command(0xC3);    //VRHS
write_data(0x1C);

write_command(0xC4);    //VDVSET
write_data(0x18);

write_command(0xC6);    //FRCTRL 2
write_data(0x0F);
write_command(0xD0);    //PWR ctrl
write_data(0xA4);
write_data(0xA2);

write_command(0xE0);    //Positive Gamma
write_data(0xF0);
write_data(0x00);

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```
write_data(0x0A);
write_data(0x10);
write_data(0x12);
write_data(0x1B);
write_data(0x39);
write_data(0x44);
write_data(0x47);
write_data(0x28);
write_data(0x12);
write_data(0x10);
write_data(0x16);
write_data(0x1B);

write_command(0x1);    //Negative Gamma
write_data(0xf0);
write_data(0x00);
write_data(0x0a);
write_data(0x10);
write_data(0x11);
write_data(0x1a);
write_data(0x3b);
write_data(0x34);
write_data(0x4e);
write_data(0x3a);
write_data(0x17);
write_data(0x16);
write_data(0x21);
write_data(0x22);

write_command(0x2A);   //Column address set
write_data(0x00);      // 0,0 --> 239
write_data(0x00);
write_data(0x00);
write_data(0xEF);

write_command(0x2B);   //Page address set
write_data(0x00);      // 0,0 --> 319
write_data(0x00);
write_data(0x01);
write_data(0x3F);

write_command(0x36);   //Memory Data Access Control
write_data(0x00);      //Top to bottom, left to right

write_command(0x3A);   //Pixel data format
write_data(0x55);      //565

write_command(0x11);   //Out of sleep
delay(120);
```

```
write_command(0x29); //Display on
write_command(0x2c); //Memory write
```

Command Descriptions

The hexadecimal commands that are in control of the display orientation are the “Memory Access Data Control” command, the “Column address set” and the “Page Address Set”. These are defined by the following display command registers.

Column Address Set

Command	Description	Value
CASET	Line length in memory	0x2A
Data 1	Start Address	0x00
Data 2		0x00
Data 3	End Address	0x00
Data 4		0xEF

The Column Address Set command is used to define the horizontal area of the display. This is also defined as line length, column length or x-axis. This will be defined by the horizontal resolution of the display. For the vertical mode, the Column Address value will be 240 pixels. The value ranges from 0 -> 239, for a total of 240 pixels in the horizontal direction. The hex representation of 239 is 0x00EF.

Row Address Set

Command	Description	Value
RASET	Frame length in memory	0x2B
Data 1	Start Address	0x00
Data 2		0x00
Data 3	End Address	0x01
Data 4		0x3f

The Row Address Set is similar to the Column Address Set command. It defines the vertical length of the frame. Together with the Row and Address set commands the area of the display can be defined. The vertical resolution is defined from 0 -> 319 which is a total of 320 pixels. This is seen as the hex command 0x013F.

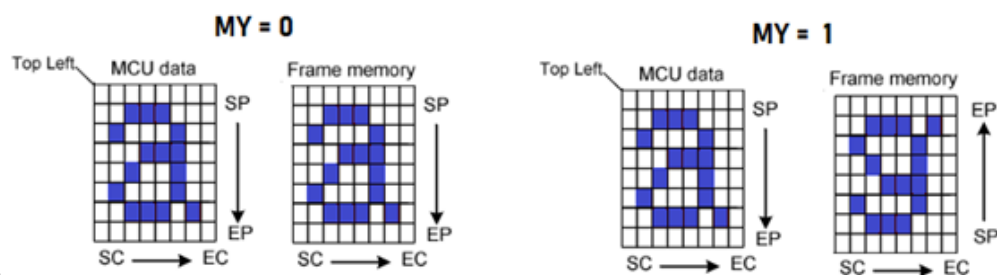
Memory Data Access Control

Command	Description								Value
MADCTL	Refresh/Scan Definition								0x36
Data	MY	MX	MV	ML	BGR	MH	X	X	--
T/B, L/R, RGB	0	0	0	0	0	0	--	--	0x00
<i>MY: Row address order</i> <i>MX: Column address order</i> <i>MV: Row/Column exchange</i> <i>ML: Vertical refresh order</i> <i>BGR: RGB-BGR order</i> <i>MH: Horizontal refresh order</i>									

The Memory Data Access Control command is the command that is in charge of changing the display orientation. This command defines the page address order, the column address order, the page/column order, and the line address order.

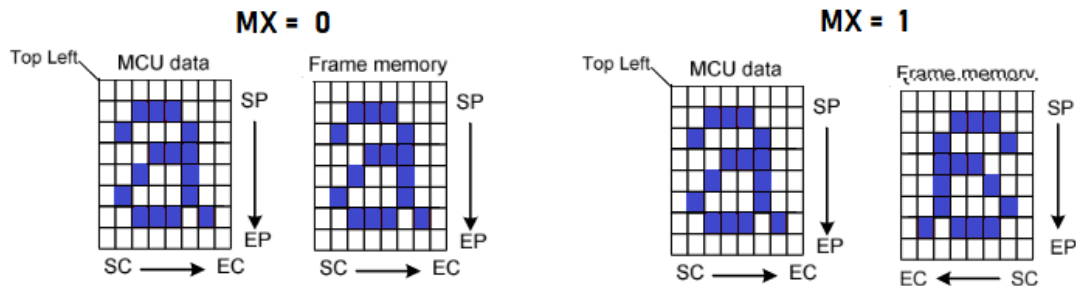
The Memory Data Access Control command, also seen as MADCTL for short, is a command that defines the read and write direction of the frame memory. This command combined with the Column and Row Address Set commands set the loading orientation of the pixel data. It can be defined to refresh the screen from top to bottom, left to right and vice versa.

The MY of the MADCTL command defines the row address order of the display. This defines the direction in which the display will update. The options for this bit are to refresh from top to bottom or bottom to top. The row address order is sometimes called the page address order or frame address order.

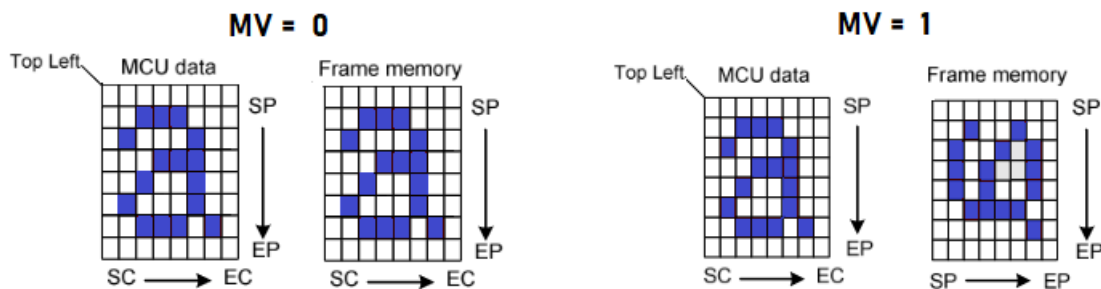


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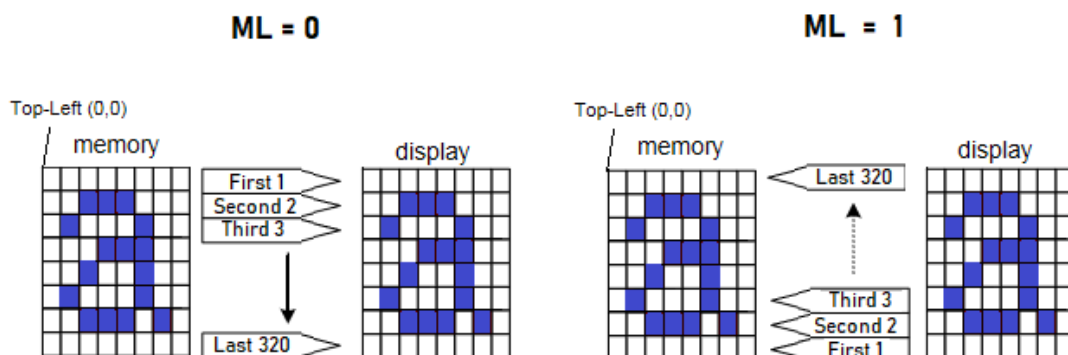
The bit that is in control of the column address order is used to define whether the display updates from right to left or from left to right. The MCU sends the data from left to right, and the frame memory of the controller will store it from right to left when $MX = 1$. When $MX = 0$, the MCU and frame memory are read from left to right. This is the standard load order seen on displays.



The row and column exchange bit is defined by MV. This switches the vertical direction and the horizontal direction. The pixel data is indicated by the MCU and is read in the frame buffer in the opposite directions.

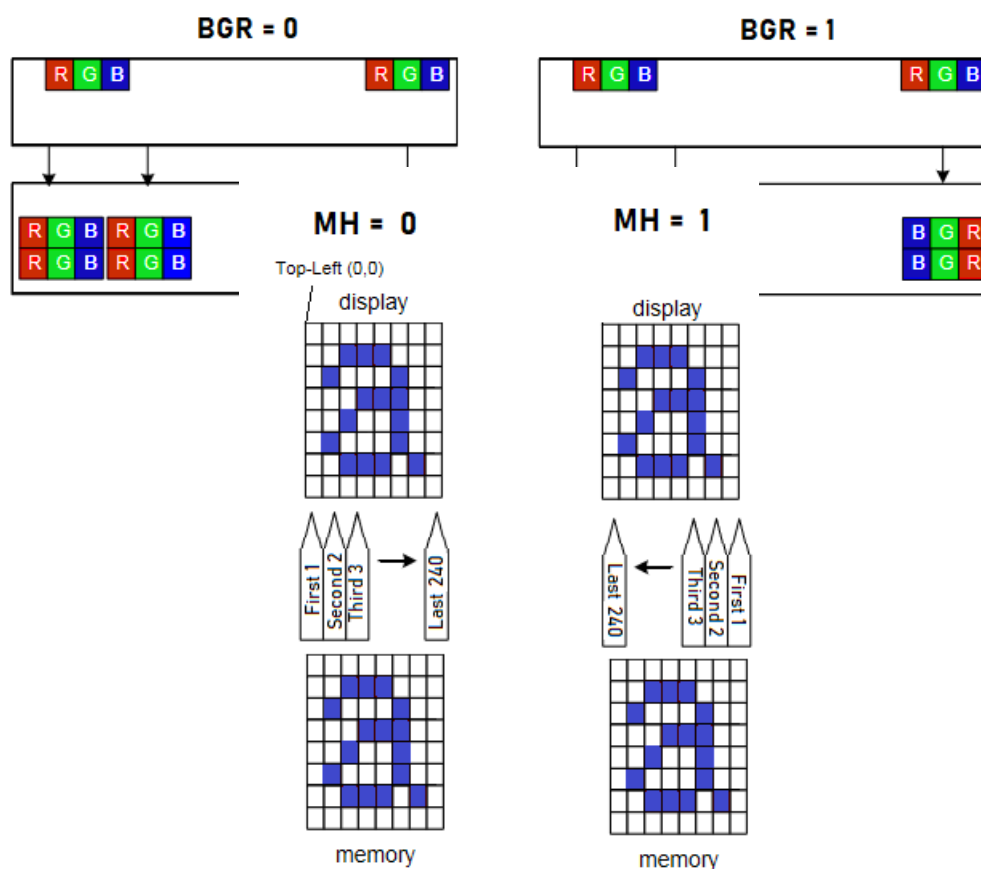


The ML value of the MADCTL command is for the vertical refresh order. This defines where the rows begin and end. This can be changed from the first row beginning at the top or bottom of the display. This will change the order in which the page begins.



The MADCTL command also defines the order of the red, blue, and green pixel data. The options for the color data are defined as R-G-B or can be switched to B-G-R through this command. This can be used to invert the color of the display by switching this bit from 0 to 1.

This bit when flipped from 0 to 1 or 1 to 0 will invert the red and blue pixel data. The green pixel data is consistent for either order. The outcome of flipping the RGB and BGR order will result in the swap of white and black as well.



The MH bit of the MADCTL command is for changing the horizontal refresh order. This bit controls the start row and end row of the pixel data frame. The rows can begin on the left and end on the right or vice versa.

Memory Access Control Visual Effects

Below are the changes in the display with changes to the memory access data register. This is to show the effect of each control bit on the display output. The MADCTL command is changed by one bit at a time to show the possible outputs and combinations. This command can be used to change the orientation of the display and switch between horizontal and vertical display modes.

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1.) Row Address Order



MY	MX	MV	ML	BGR	MH	Hex
0	0	0	0	0	0	0x00



MY	MX	MV	ML	BGR	MH	Hex
1	0	0	0	0	0	0x80

2.) Column Address Order



MY	MX	MV	ML	BGR	MH	Hex
0	0	0	0	0	0	0x00



MY	MX	MV	ML	BGR	MH	Hex
0	1	0	0	0	0	0x40

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3.) Row/Column Exchange



MY	MX	MV	ML	BGR	MH	Hex
0	0	0	0	0	0	0x00



MY	MX	MV	ML	BGR	MH	Hex
0	0	1	0	0	0	0x20

4.) Row/Column Exchange with MY = 1



MY	MX	MV	ML	BGR	MH	Hex
0	0	0	0	0	0	0x00



MY	MX	MV	ML	BGR	MH	Hex
1	0	1	0	0	0	0xA0

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